

NALAA

Hamburg 10

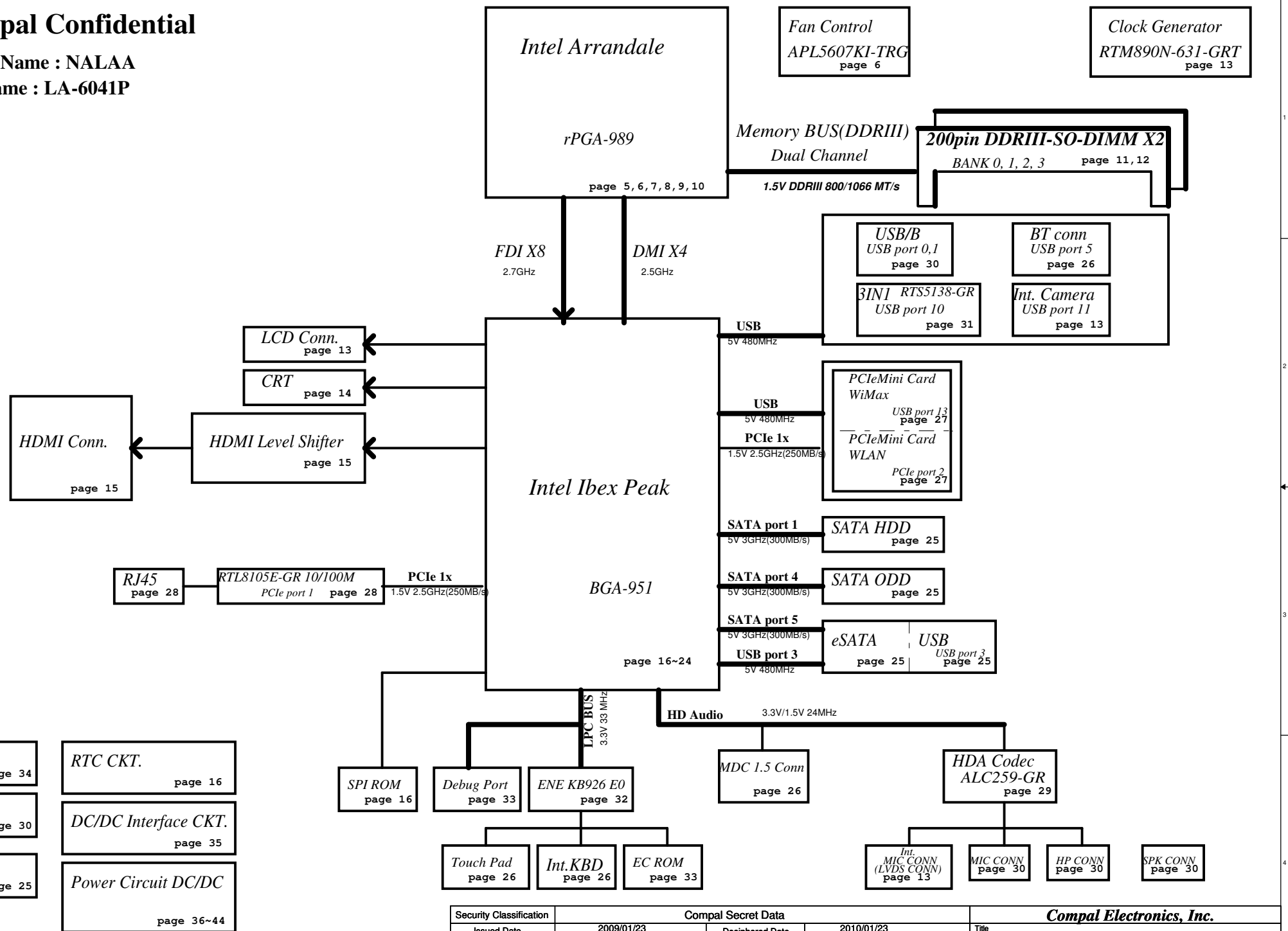
LA-6041P REV 1.0 Schematic

Intel Arrandale /IBEX PEAK

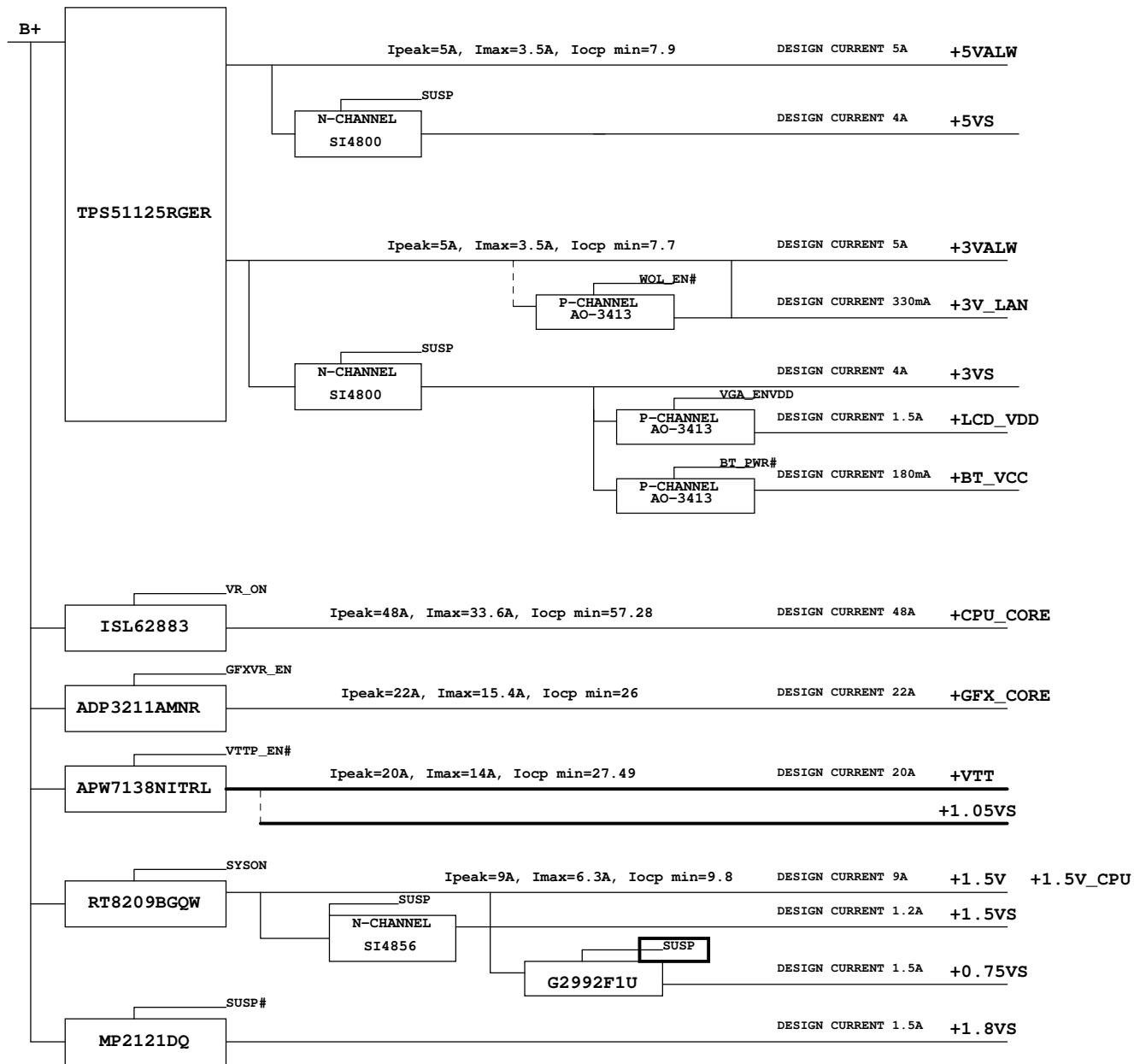
2009-10-01 Rev 1.0

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				Cover Page	
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Model Name : NALAA
File Name : LA-6041P



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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title Block Diagrams				
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	RJ11	LAN	HDMI	Card Reader	Express Card		Mini Card
description	(B)	(R)	(E)	(Y)	(W)			
explain	Bluetooth	MDC	LAN	HDMI	Card Reader	New Card	PCMCIA	WIRELESS
BTO	BT@	MDC@		IHDMI@	CARD@			WLAN@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

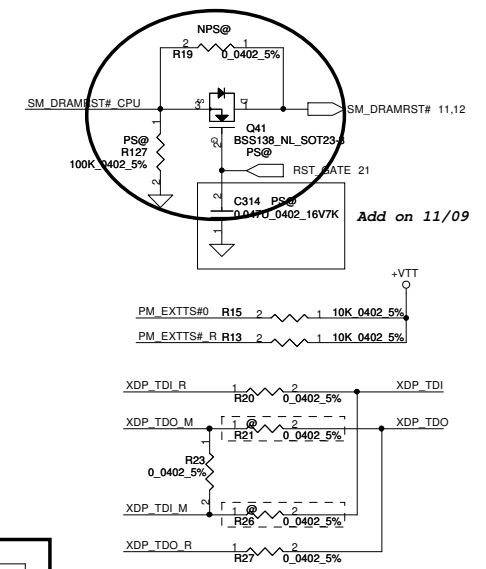
EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VS	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b	+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
			+3VS	PCH	0100 110x b

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

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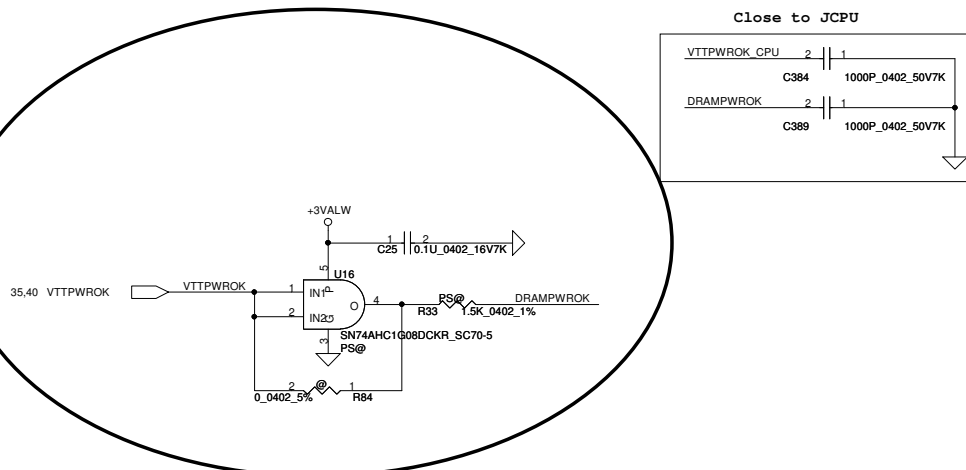
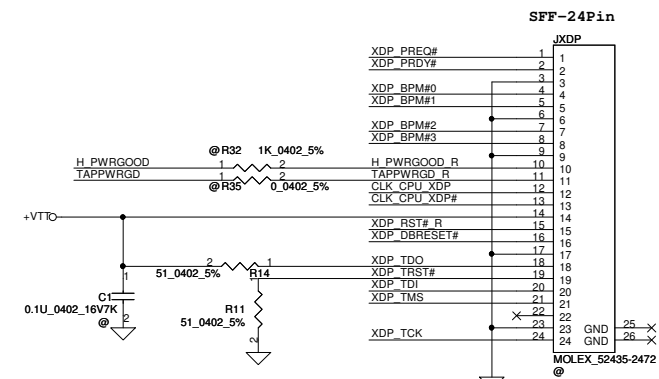


Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

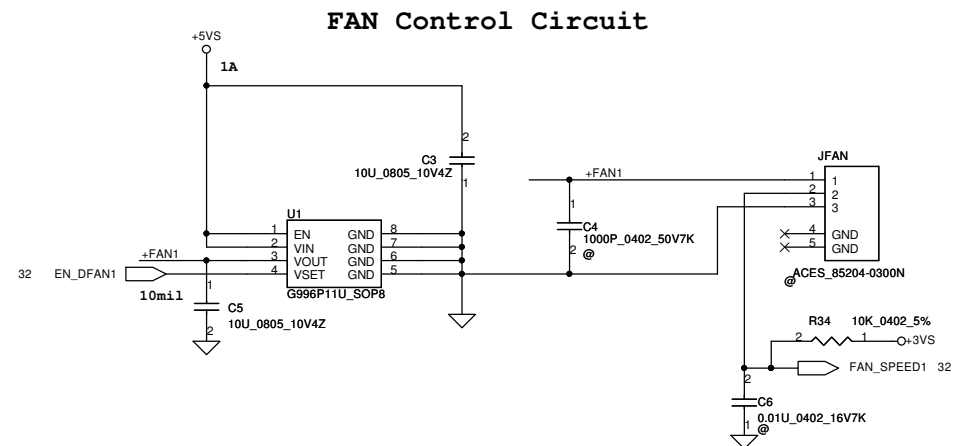
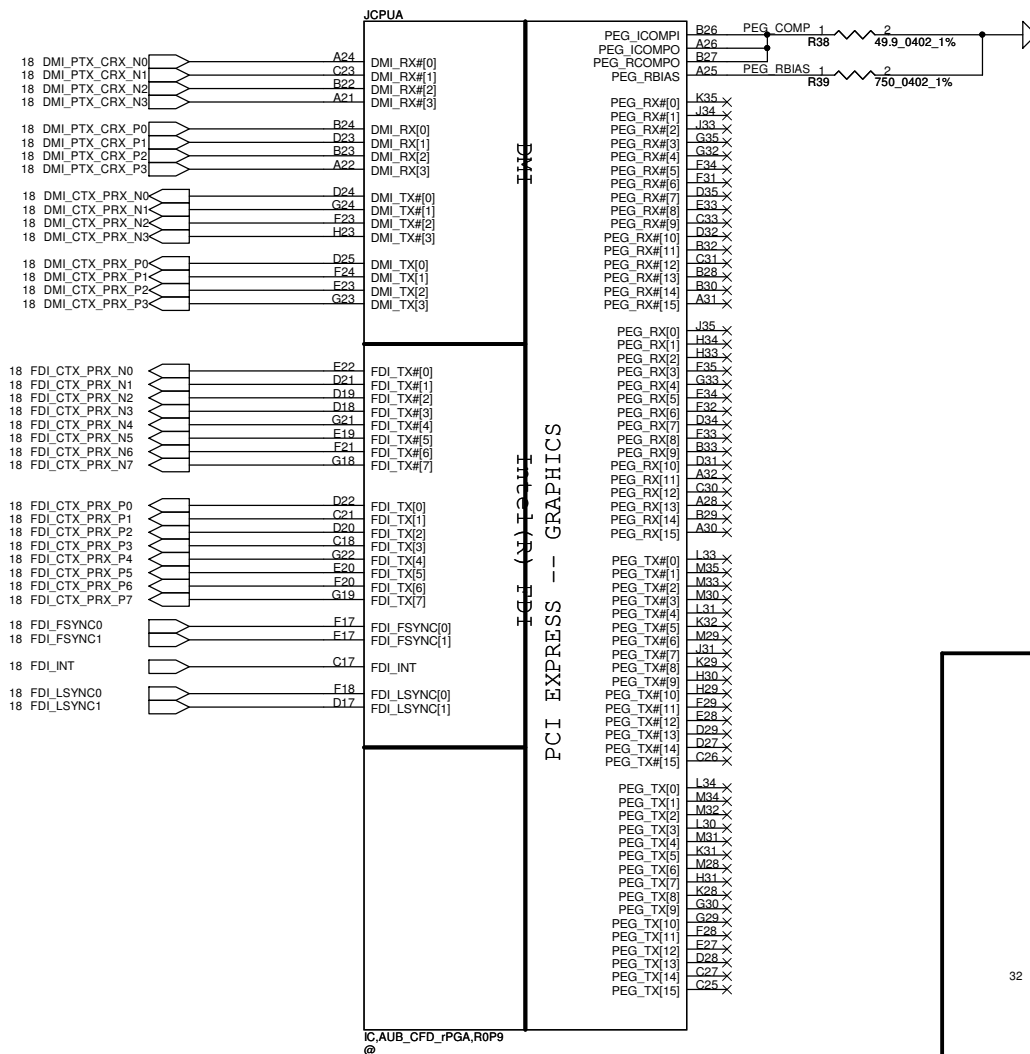
EMI reverse, close to JCPU

XDP_PRDY#	C7	2	0.1U_0402_10V6K
XDP_FREQ#	C8	2	0.1U_0402_10V6K
XDP_TCK	C9	2	0.1U_0402_10V6K
XDP_TMS	C10	2	0.1U_0402_10V6K
XDP_TRST#	C11	2	0.1U_0402_10V6K
XDP_TDI_R	C12	2	0.1U_0402_10V6K
XDP_TDO_R	C13	2	0.1U_0402_10V6K
XDP_TDI_M	C14	2	0.1U_0402_10V6K
XDP_TDO_M	C15	2	0.1U_0402_10V6K
XDP_DBRESET#	C17	2	0.1U_0402_10V6K

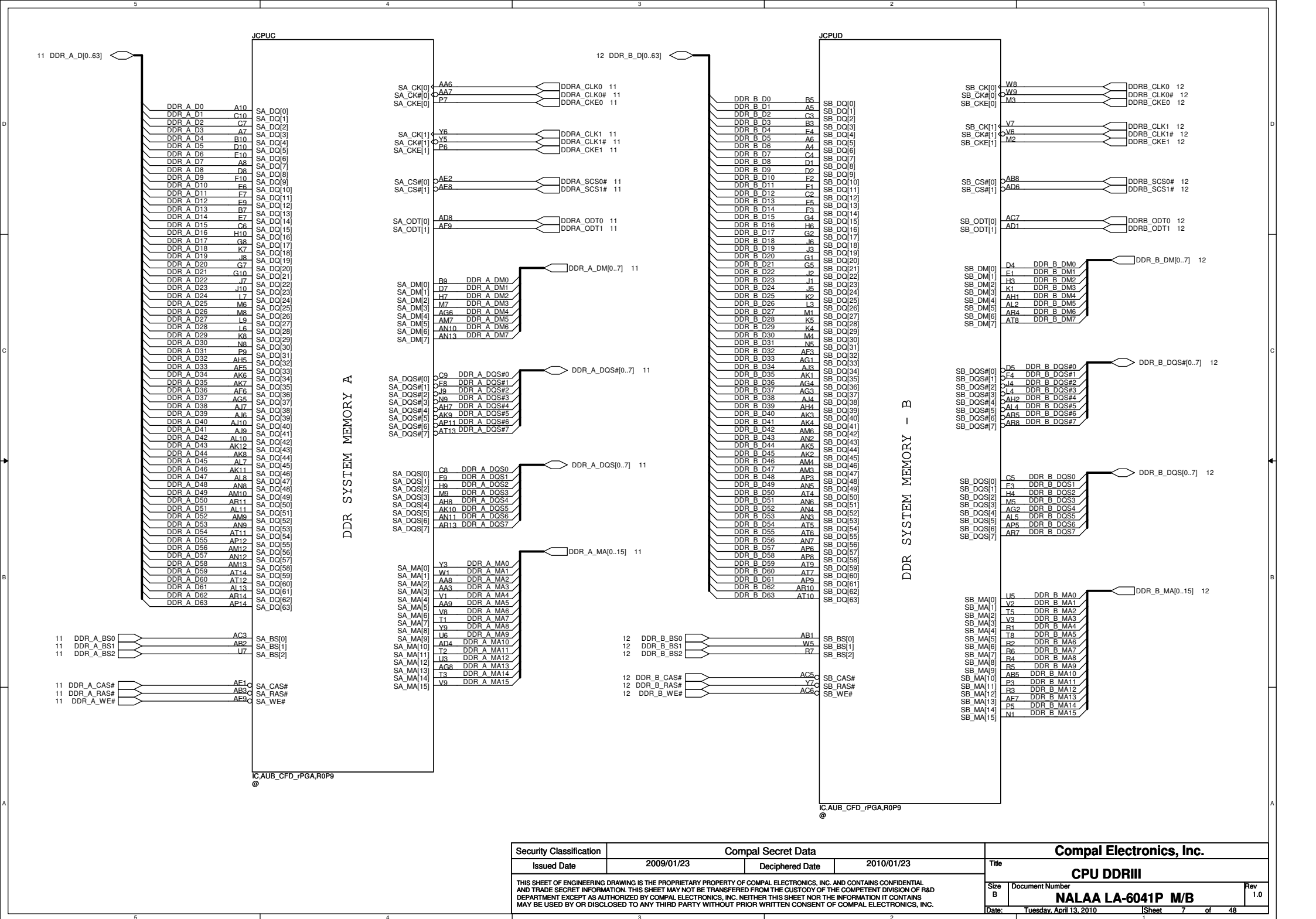
XDP Connector

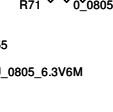
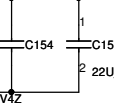
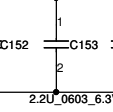
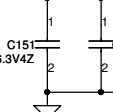
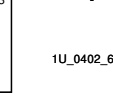
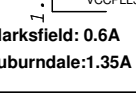
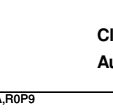
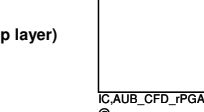
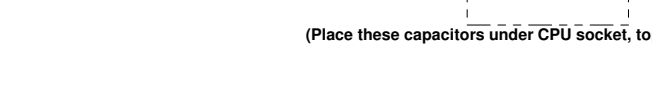
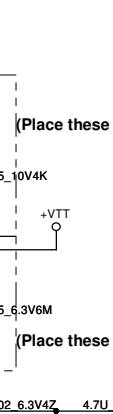
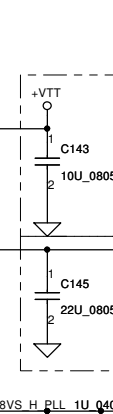
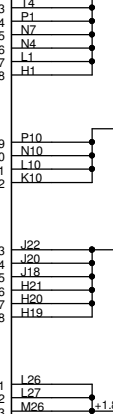
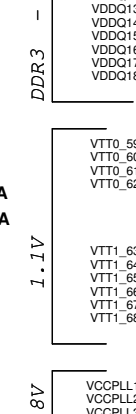
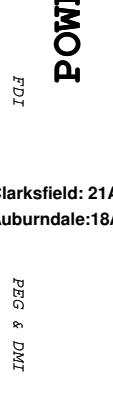
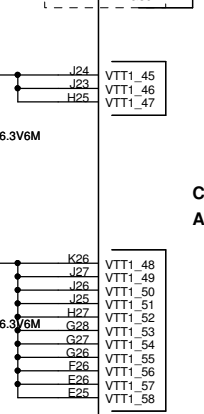
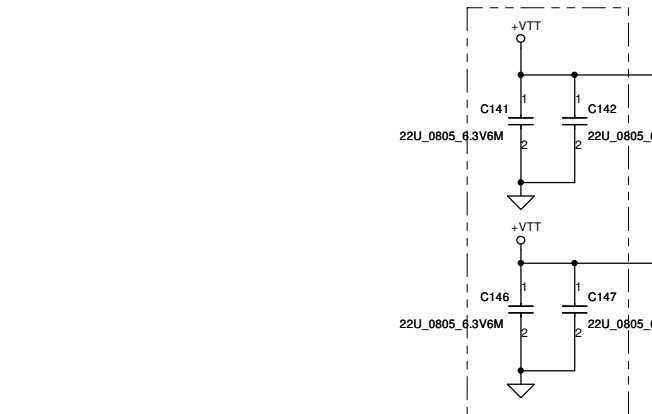
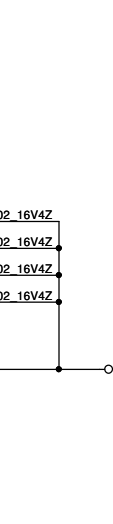
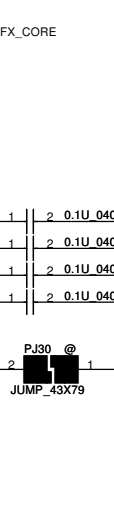
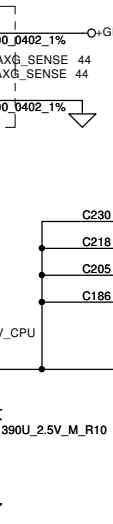
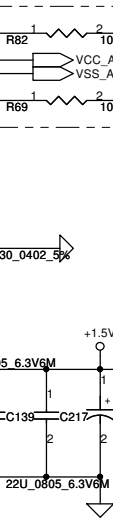
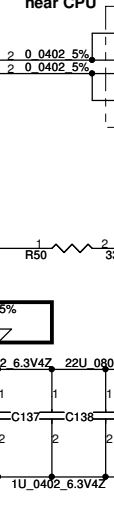
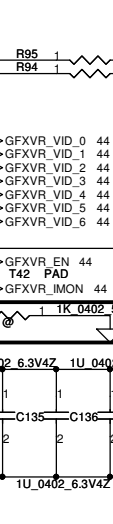
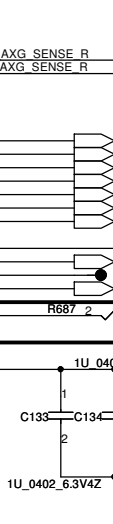
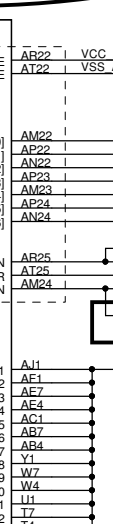
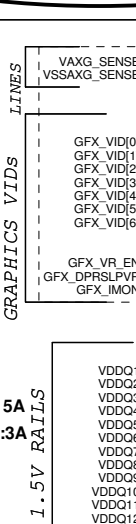
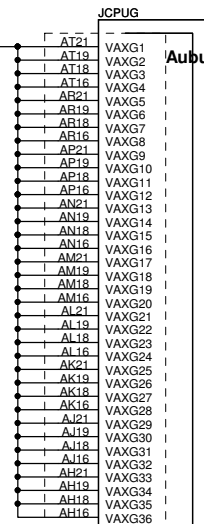
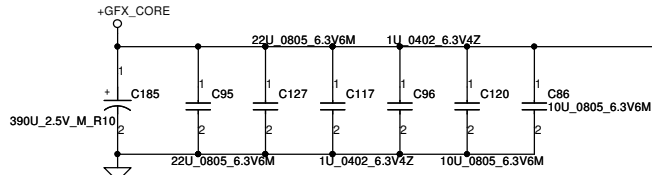
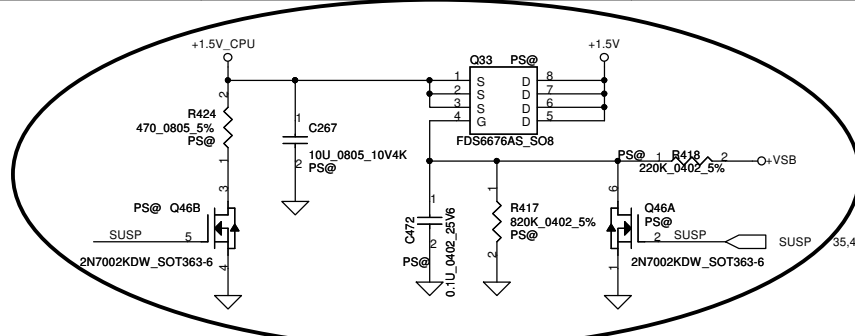
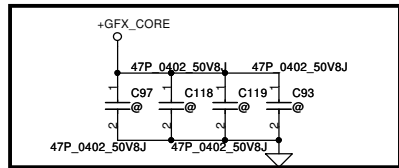


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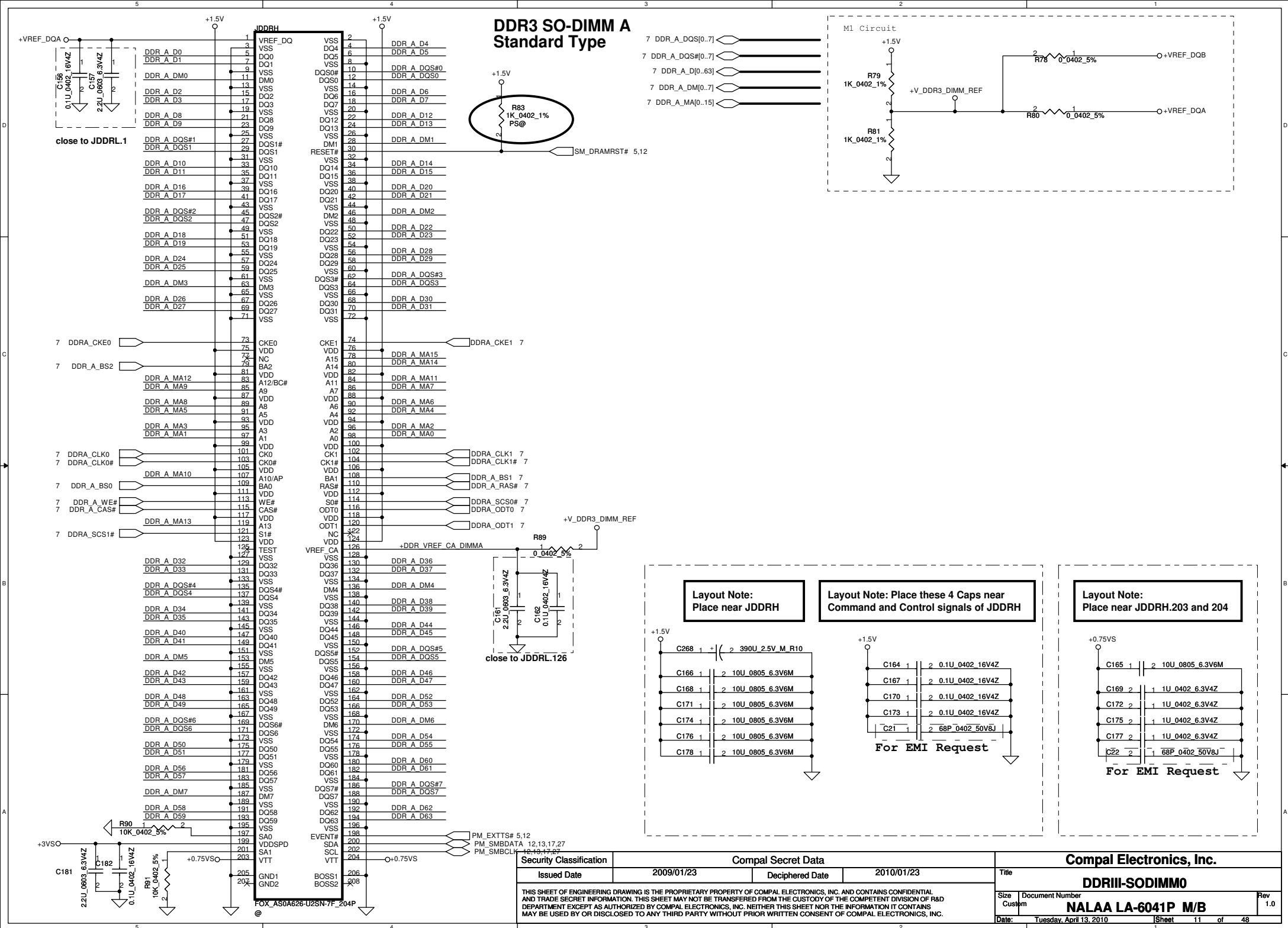


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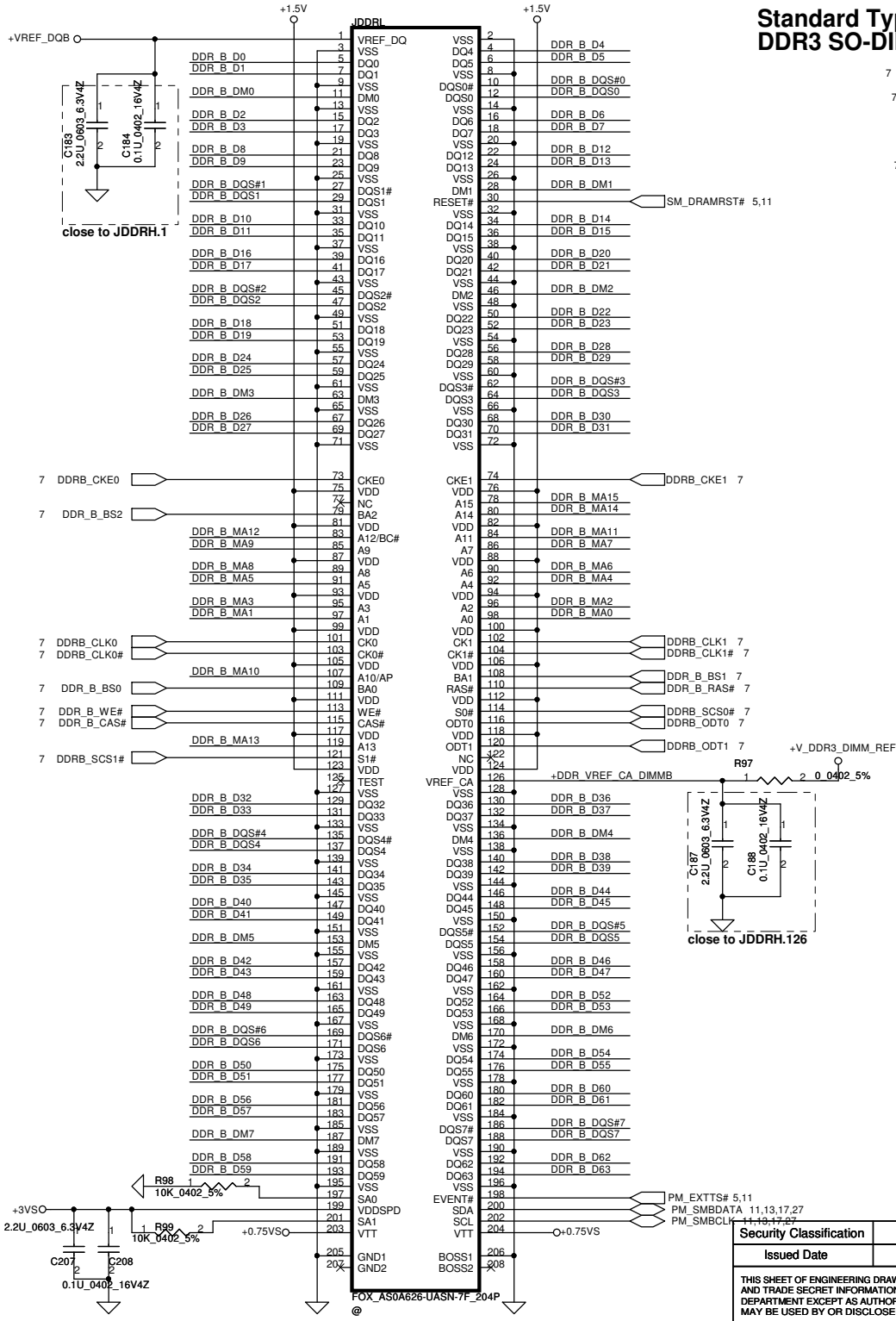




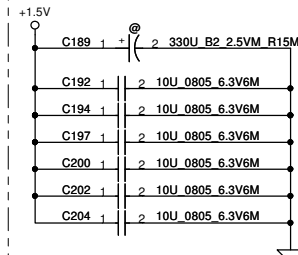
Security Classification	
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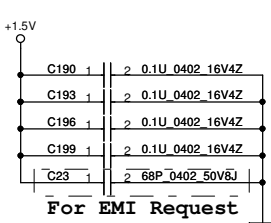
Standard Type DDR3 SO-DIMM B



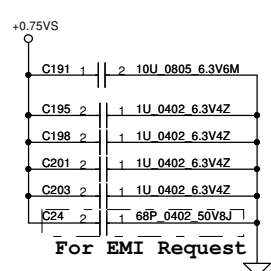
Layout Note:
Place near JDDR1



Layout Note: Place these 4 Caps near
Command and Control signals of JEERL



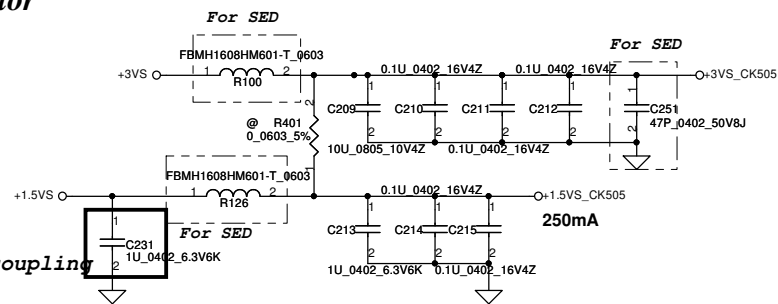
Layout Note:
Place near JDDR1.203 and 204



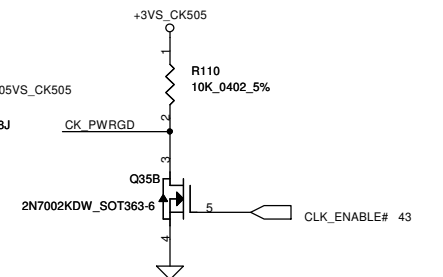
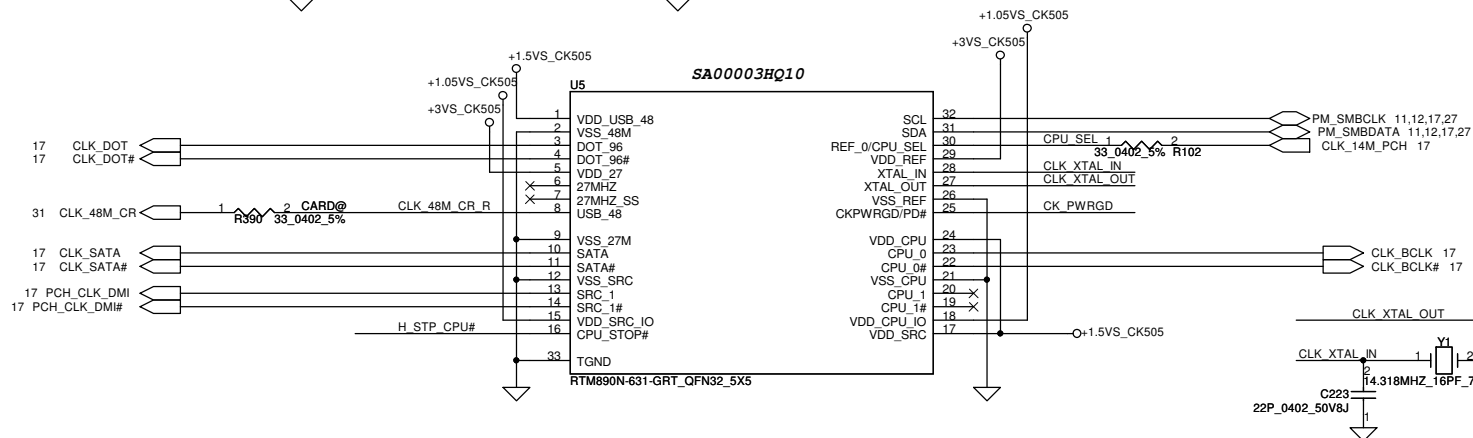
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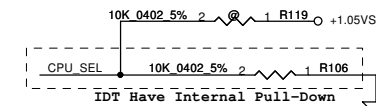
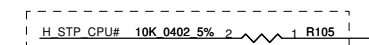
Clock Generator



Prevent noise coupling



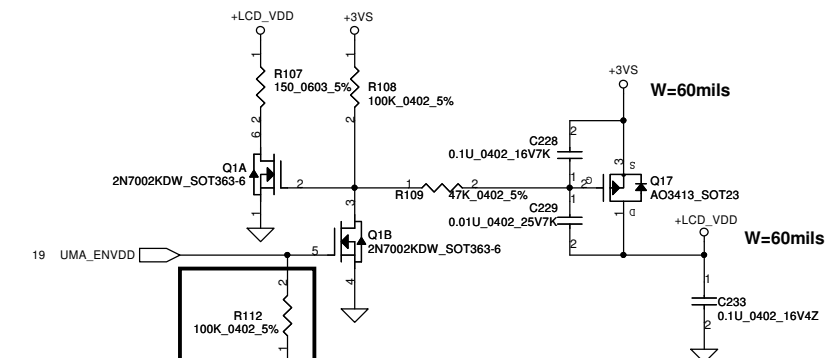
Silego Have Internal Pull-Up



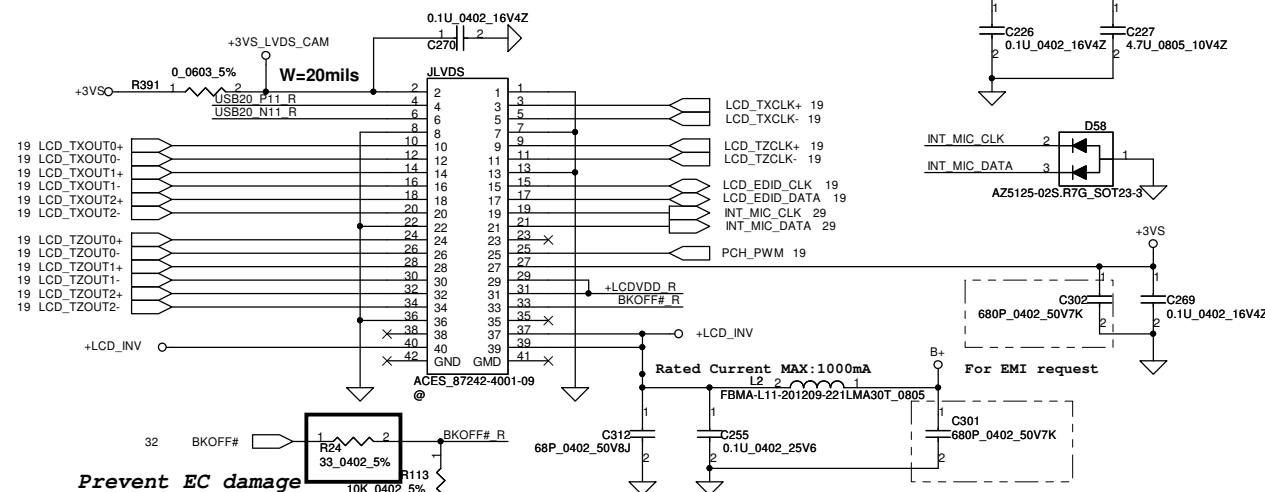
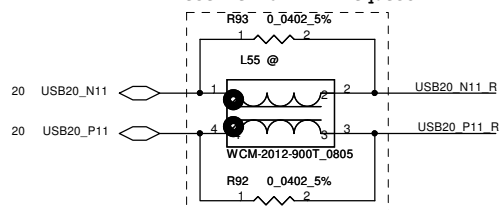
CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Routing the
trace at
least 10mil

LCD/PANEL BD. Conn.

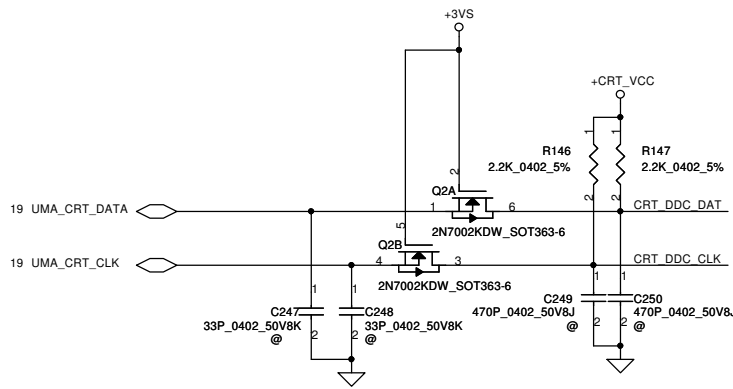
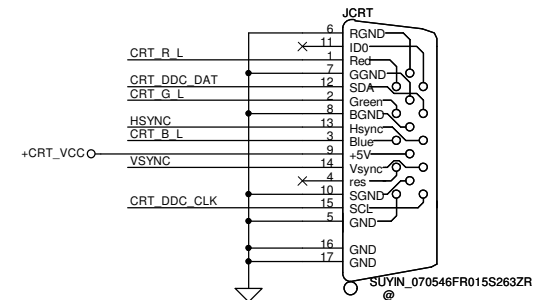
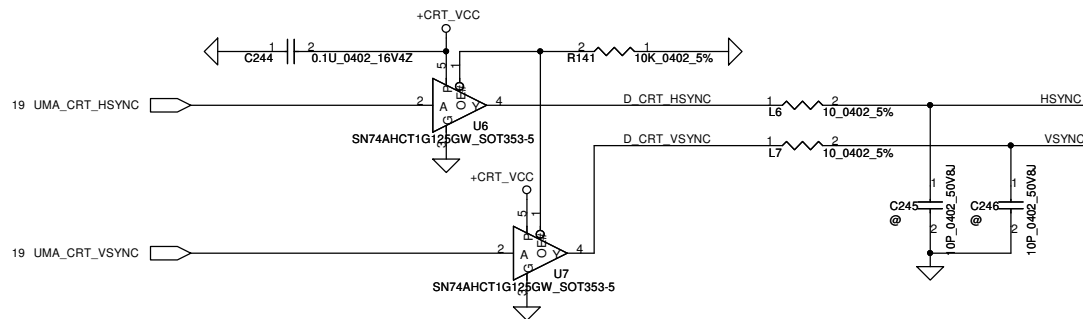
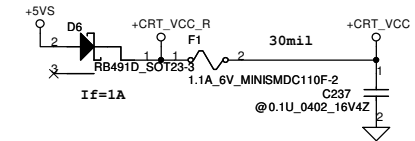
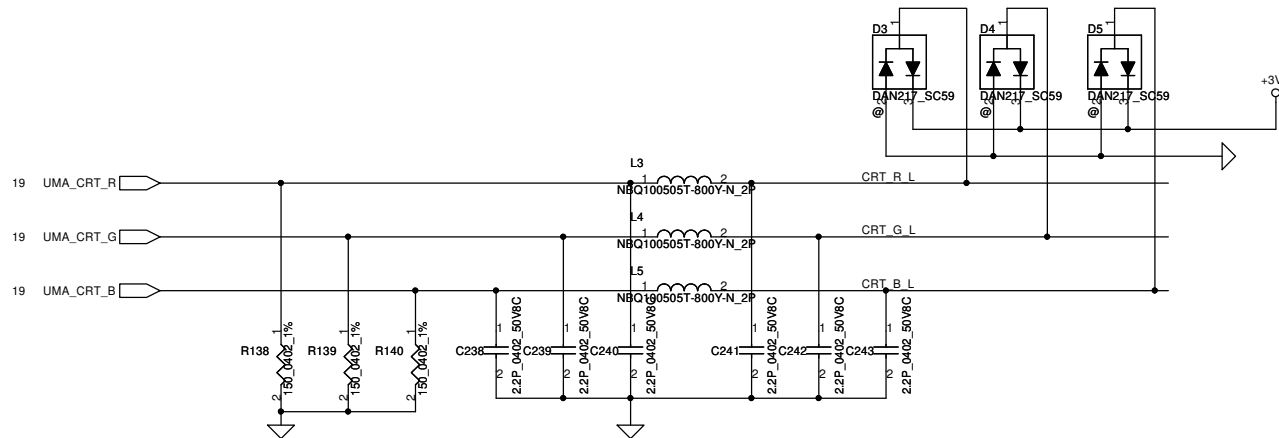


Reserve for EMI request

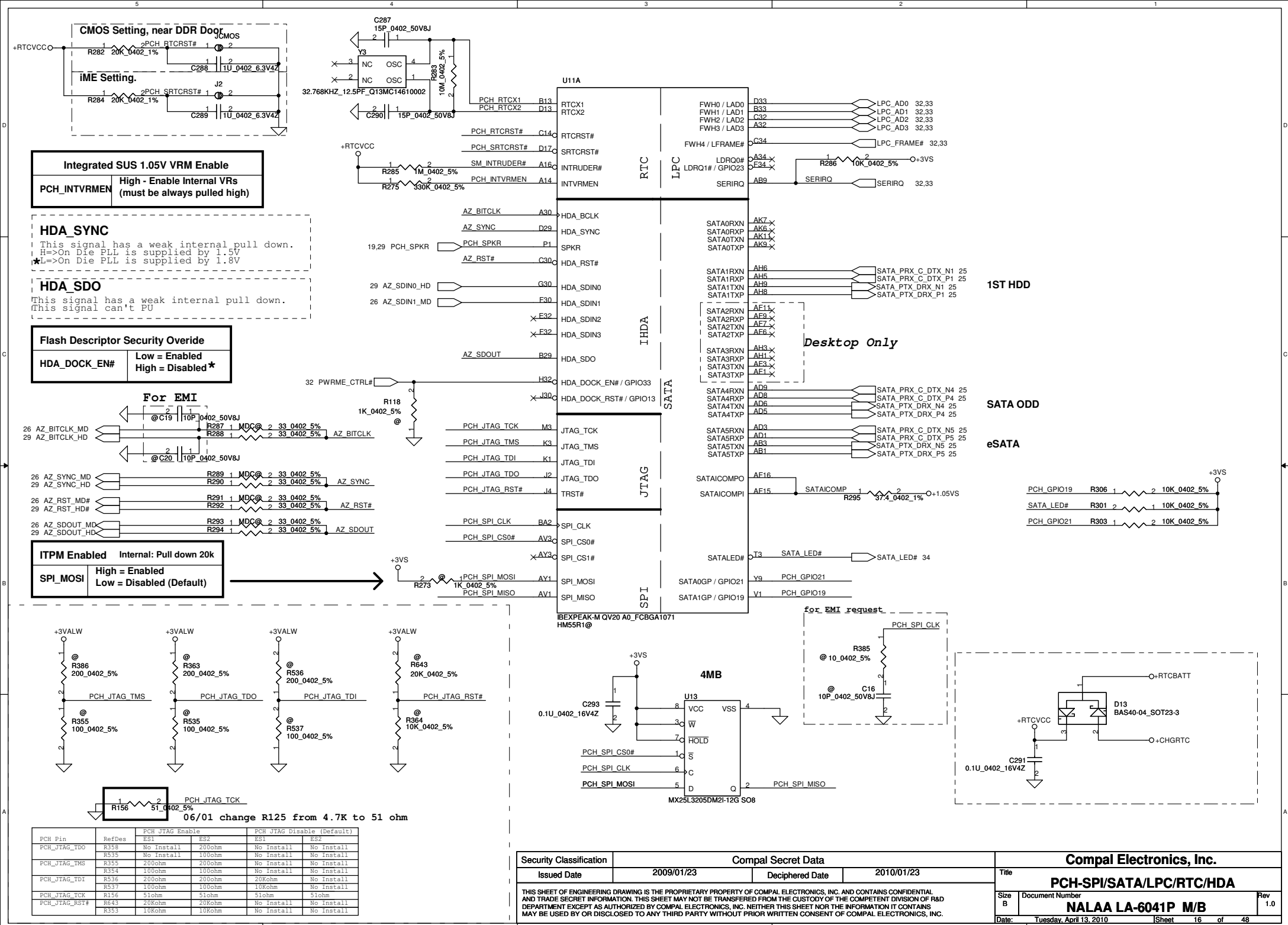


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CRT CONNECTOR



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For LAN

28 PCIE_PRX_C_LANTX_N1
28 PCIE_PRX_C_LANTX_P1
28 PCIE_PTX_C_LANRX_N1
28 PCIE_PTX_C_LANRX_P1

For WLAN

27 PCIE_PRX_WLANTX_N2
27 PCIE_PRX_WLANTX_P2
27 PCIE_PTX_C_WLANRX_N2
27 PCIE_PTX_C_WLANRX_P2

LAN

28 CLK_LAN#
28 CLK_LAN
28 CLKREQ_LAN#

WLAN

27 CLK_WLAN#
27 CLK_WLAN
27 CLKREQ_WLAN#

PCH_GPIO20
PCH_GPIO25
PCH_GPIO26
PCH_GPIO44
PCH_GPIO56
PCH_GPIO20
PCH_GPIO25
PCH_GPIO26
PCH_GPIO44
PCH_GPIO56

U11B

NC

PCI-E*

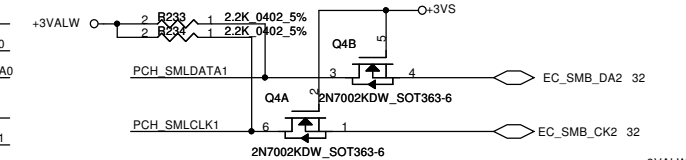
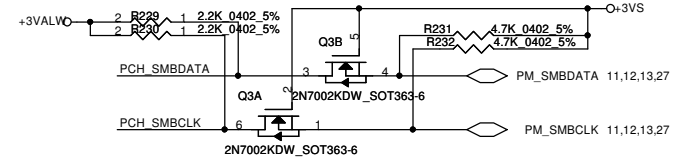
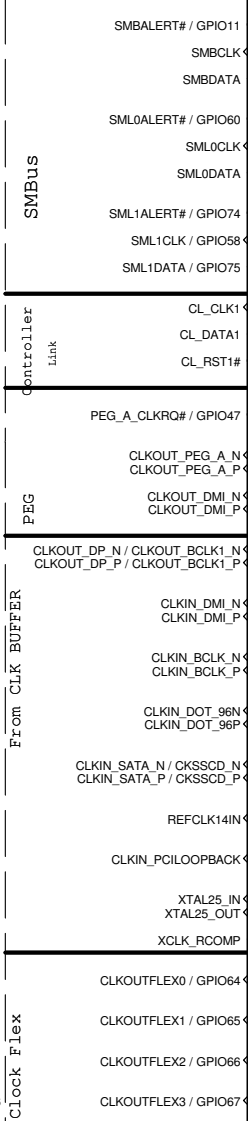
Controller Link

PEG

From CLK BUFFER

Clock Flex

BEXPEAK-M QV20 A0_FCBGA1071
HM55R1@



PCH_SMLCLK0 2.2K 0402_5% 2 R237
PCH_SMLDATA0 2.2K 0402_5% 2 R238
PCH_GPIO60 10K 0402_5% 2 R239
PCH_GPIO74 10K 0402_5% 2 R240
EC_LID_OUT# 10K 0402_5% 2 R241

CLKREQ_PEG# 1 R260 10K_0402_5% +3VALW

CLK_PEG# 5
CLK_PEG 5

PCH_CLK_DMI# 13
PCH_CLK_DMI 13

CLK_BCLK# 13
CLK_BCLK 13

CLK_DOT# 13
CLK_DOT 13

CLK_SATA# 13
CLK_SATA 13

CLK_14M_PCH 13

CLK_PCIL0P 20

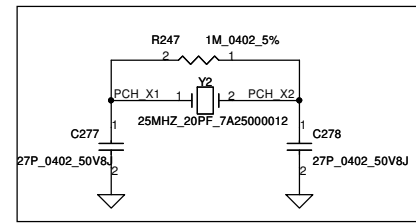
CLK_14M_PCH 13

CLK_PCIL0P 20

CLK_14M_PCH 13

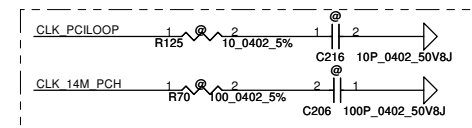
CLK_PCIL0P 20

FROM CLK GEN FOR: 133/100/96/14.318 MHZ

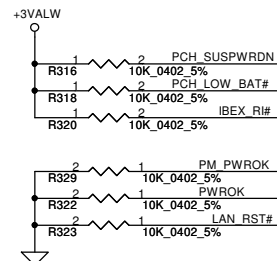


Note: Stuff 0 ohm if 25MHZ crystal un-stuff

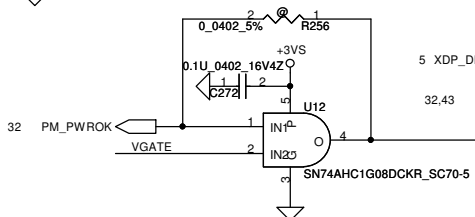
for EMI request



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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	CLK/PCIE/SMBUS
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				NALAA LA-6041P M/B	
				Date	Tuesday, April 13, 2010
				Sheet	17 of 48
				Rev	1.0



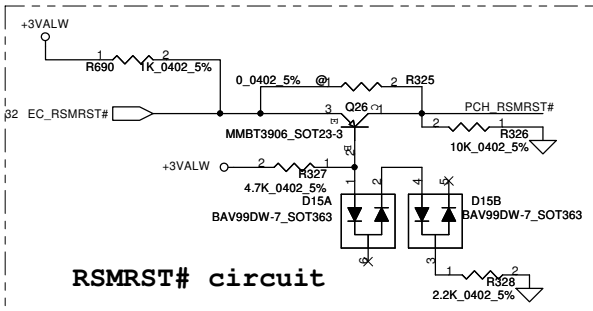
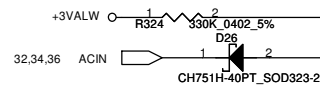
Close to PCH



LAN_RST#

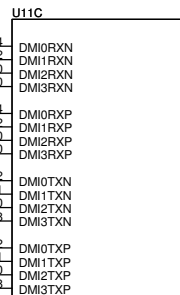
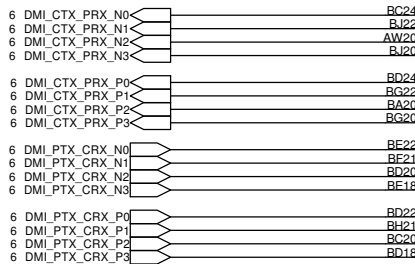
PCH_SUSPWRDN

PBTN_OUT#



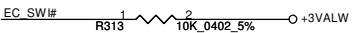
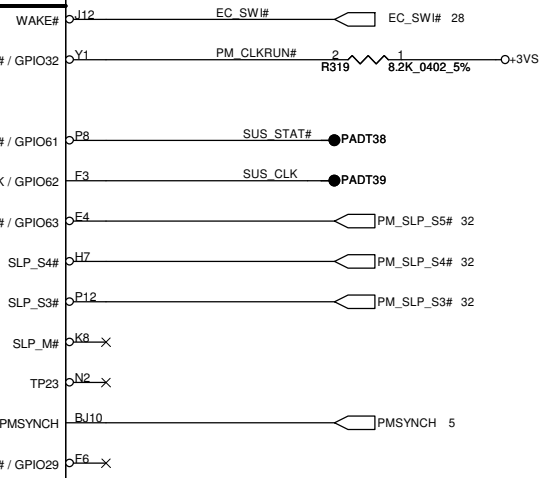
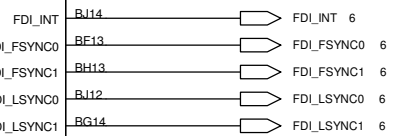
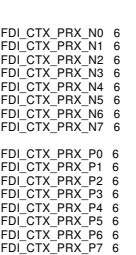
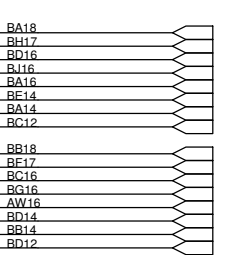
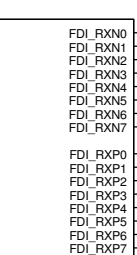
RSMRST# circuit

U11C



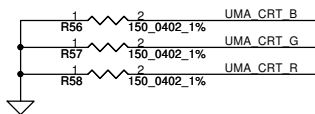
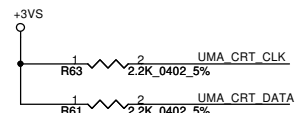
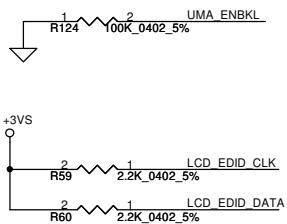
DMI

System Power Management

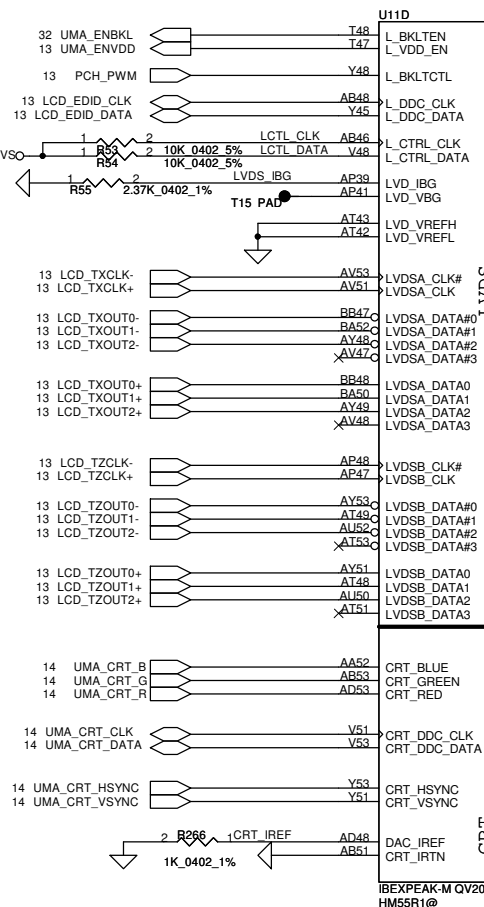
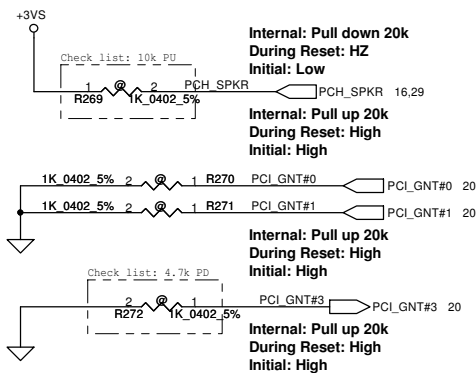


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/01/23				Deciphered Date			
2009/01/23				2010/01/23				Title			
								PCH-DMI/FDI/PWM			
Size				Document Number				Rev			
B				NALAA LA-6041P M/B				1.0			
Date:				Tuesday, April 13, 2010				Sheet			
								18 of 48			

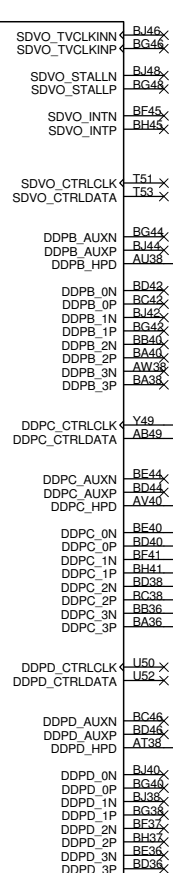
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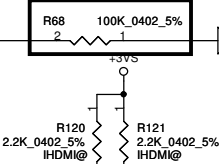
PCH Strap Pin



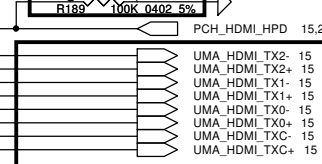
Digital Display Interface



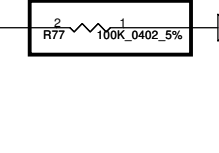
For INTEL issue (pending interrupts from the PCH for unused HDMI ports)



For INTEL issue (pending interrupts from the PCH for unused HDMI ports)



For INTEL issue (pending interrupts from the PCH for unused HDMI ports)



HDMI

NO REBOOT Strap

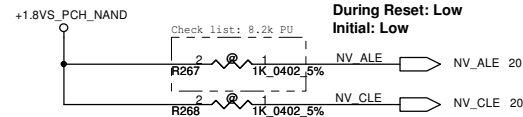
PCH_SPKR	Low= Disable High= Enable
----------	------------------------------

Boot BIOS Strap

PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable
-----------	--



Internal: Pull down 20k
During Reset: Low
Initial: Low

Internal: Pull down 20k
During Reset: Low
Initial: Low

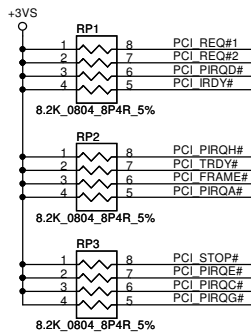
Danbury Technology Enabled

NV_ALE	High = Enabled Low = Disabled (Default)
--------	--

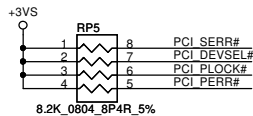
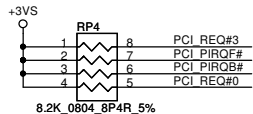
DMI Termination Voltage

NV_CLE	Low= Set to Vss (Default) High= Set to Vcc
--------	---

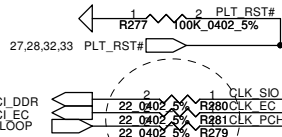
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Size	Document Number	Rev		1.0
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Date:	Tuesday, April 13, 2010	Sheet	19	of 48



GNT2#: Not pull low, internal pull up 20K



33 CLK_PCI_DDR
32 CLK_PCI_EC
17 CLK_PCI_LOOP



Change to 47 ohm?

PCI_PIRQA# G38C
PCI_PIRQB# H51C
PCI_PIRQC# B37C
PCI_PIRQD# A44C
PCI_REQ#0 F51C
PCI_REQ#1 A46C
PCI_REQ#2 B45C
PCI_REQ#3 M53C

PCI_PIRQE# B41C
PCI_PIRQF# K53C
PCI_PIRQG# A36C
PCI_PIRQH# A48C

PCI_IRDY# A42C
PCI_DEVSEL# H44C
PCI_FRAME# F46C
PCI_PLOCK# D49C

PCI_STOP# D41C
PCI_TRDY# C48C

CLKOUT_PCI0 N52
CLKOUT_PCI1 P53
CLKOUT_PCI2 P46
CLKOUT_PCI3 P51
CLKOUT_PCI4 P48

U11E

AD0 H40
AD1 N34
AD2 C44
AD3 A38
AD4 J34
AD5 A40
AD6 D45
AD7 E36
AD8 H48
AD9 E40
AD10 C40
AD11 M48
AD12 M45
AD13 F53
AD14 M40
AD15 M42
AD16 J36
AD17 K46
AD18 E40
AD19 C42
AD20 K46
AD21 M51
AD22 M52
AD23 K51
AD24 L34
AD25 F42
AD26 J40
AD27 G46
AD28 F44
AD29 M47
AD30 K36
AD31 J36

C/BE0# J50C
C/BE1# G42C
C/BE2# H47C
C/BE3# G34C

PIROA# G38C
PIROB# H51C
PIROC# B37C
PIQD# A44C

REQ0# F51C
REQ1# / GPIO50 A46C
REQ2# / GPIO52 B45C
REQ3# / GPIO54 M53C

GNT0# F48C
GNT1# / GPIO51 K45C
GNT2# / GPIO53 E36C
GNT3# / GPIO55 H53C

PIRQE# B41C
PIROF# K53C
PIROG# A36C
PIROH# A48C

TP PCI_RST# K6C
SERR# F44C
PERR# E50C

IRDY# A42C
PAR F44C
DEVSEL# F46C
FRAME# C46C

PLOCK# D49C
STOP# D41C
TRDY# C48C

PME# M7C
PLTRST# D5C

CLKOUT_PCI0 N52
CLKOUT_PCI1 P53
CLKOUT_PCI2 P46
CLKOUT_PCI3 P51
CLKOUT_PCI4 P48

IBEXPEAK-M QV20 A0_FCBGA1071
HM55R1@

PCI

NVRAM

NV_CE#0 AY9
NV_CE#1 BD1
NV_CE#2 AP15
NV_CE#3 BD8
NV_DQS0 AV9
NV_DQS1 BG8
NV_DQ0 / NV_IO0 AP7
NV_DQ1 / NV_IO1 AP6
NV_DQ2 / NV_IO2 AT6
NV_DQ3 / NV_IO3 A19
NV_DQ4 / NV_IO4 BB1
NV_DQ5 / NV_IO5 AV6
NV_DQ6 / NV_IO6 BB3
NV_DQ7 / NV_IO7 BA4
NV_DQ8 / NV_IO8 BE4
NV_DQ9 / NV_IO9 BE6
NV_DQ10 / NV_IO10 BB7
NV_DQ11 / NV_IO11 BC8
NV_DQ12 / NV_IO12 BJ8
NV_DQ13 / NV_IO13 BJ6
NV_DQ14 / NV_IO14 BG6
NV_DQ15 / NV_IO15

NV_ALE BD3
NV_CLE AY6

NV_RCOMP AU2
NV_RB# AV7

NV_WR#0_RE# AV8
NV_WR#1_RE# AY5
NV_WE#_CK0 AV11
NV_WE#_CK1 BF5

USBP0N H18
USBP0P J18
USBP1N A18
USBP1P C18
USBP2N N20
USBP2P P20
USBP3N J20
USBP3P L20
USBP4N F20
USBP4P A20
USBP5N C20
USBP5P M22
USBP6N N22
USBP6P B21
USBP7N B21
USBP7P D21
USBP8N H22
USBP8P J22
USBP9N E22
USBP9P F22
USBP10N A22
USBP10P C22
USBP11N G24
USBP11P H24
USBP12N L24
USBP12P M24
USBP13N A24
USBP13P C24

USB20_N0 30
USB20_P0 30
USB20_N1 30
USB20_P1 30
USB20_N3 25
USB20_P3 25
USB20_N5 26
USB20_P5 26

USB20_N10 31
USB20_P10 31
USB20_N11 13
USB20_P11 13
USB20_N13 27
USB20_P13 27

USBRBIAS# B25
USBRBIAS D25

USBBIAS R278
Within 500 mils

OC0# / GPIO59 N16
OC1# / GPIO40 J16
OC2# / GPIO41 E16
OC3# / GPIO42 L16
OC4# / GPIO43 E14
OC5# / GPIO49 G16
OC6# / GPIO10 F12
OC7# / GPIO14 C15

USB_OC#0 N16
USB_OC#1 J16
USB_OC#2 E16
USB_OC#3 L16
USB_OC#4 E14
USB_OC#5 G16
USB_OC#6 F12
EXP_CPPE# C15

USB_OC#0 30,32
USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

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USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

NV_CE#0 AY9
NV_CE#1 BD1
NV_CE#2 AP15
NV_CE#3 BD8
NV_DQS0 AV9
NV_DQS1 BG8
NV_DQ0 / NV_IO0 AP7
NV_DQ1 / NV_IO1 AP6
NV_DQ2 / NV_IO2 AT6
NV_DQ3 / NV_IO3 A19
NV_DQ4 / NV_IO4 BB1
NV_DQ5 / NV_IO5 AV6
NV_DQ6 / NV_IO6 BB3
NV_DQ7 / NV_IO7 BA4
NV_DQ8 / NV_IO8 BE4
NV_DQ9 / NV_IO9 BE6
NV_DQ10 / NV_IO10 BB7
NV_DQ11 / NV_IO11 BC8
NV_DQ12 / NV_IO12 BJ8
NV_DQ13 / NV_IO13 BJ6
NV_DQ14 / NV_IO14 BG6
NV_DQ15 / NV_IO15

NV_ALE BD3
NV_CLE AY6

NV_RCOMP AU2
NV_RB# AV7

NV_WR#0_RE# AV8
NV_WR#1_RE# AY5
NV_WE#_CK0 AV11
NV_WE#_CK1 BF5

USBP0N H18
USBP0P J18
USBP1N A18
USBP1P C18
USBP2N N20
USBP2P P20
USBP3N J20
USBP3P L20
USBP4N F20
USBP4P A20
USBP5N C20
USBP5P M22
USBP6N N22
USBP6P B21
USBP7N B21
USBP7P D21
USBP8N H22
USBP8P J22
USBP9N E22
USBP9P F22
USBP10N A22
USBP10P C22
USBP11N G24
USBP11P H24
USBP12N L24
USBP12P M24
USBP13N A24
USBP13P C24

USB20_N0 30
USB20_P0 30
USB20_N1 30
USB20_P1 30
USB20_N3 25
USB20_P3 25
USB20_N5 26
USB20_P5 26

USB20_N10 31
USB20_P10 31
USB20_N11 13
USB20_P11 13
USB20_N13 27
USB20_P13 27

USBRBIAS# B25
USBRBIAS D25

USBBIAS R278
Within 500 mils

OC0# / GPIO59 N16
OC1# / GPIO40 J16
OC2# / GPIO41 E16
OC3# / GPIO42 L16
OC4# / GPIO43 E14
OC5# / GPIO49 G16
OC6# / GPIO10 F12
OC7# / GPIO14 C15

USB_OC#0 N16
USB_OC#1 J16
USB_OC#2 E16
USB_OC#3 L16
USB_OC#4 E14
USB_OC#5 G16
USB_OC#6 F12
EXP_CPPE# C15

USB_OC#0 30,32
USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

USB_OC#0 30,32
USB_OC#1 25,32

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USB_OC#0 30,32
USB_OC#1 25,32

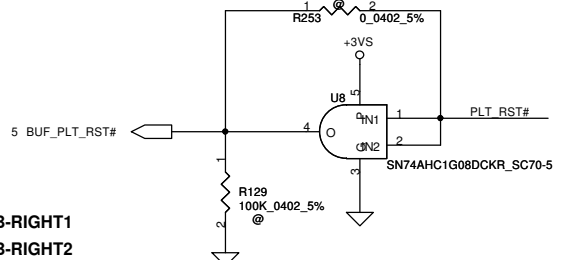
USB-RIGHT1
USB-RIGHT2

eSATA-USB

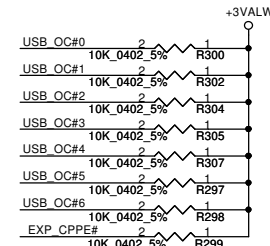
BT

Card reader(3 in 1)
Int. Camera

WLAN



Within 500 mils



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				Date: Tuesday, April 13, 2010	Sheet 20 of 48
				Rev 1.0	

GPIO8

Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15

a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR

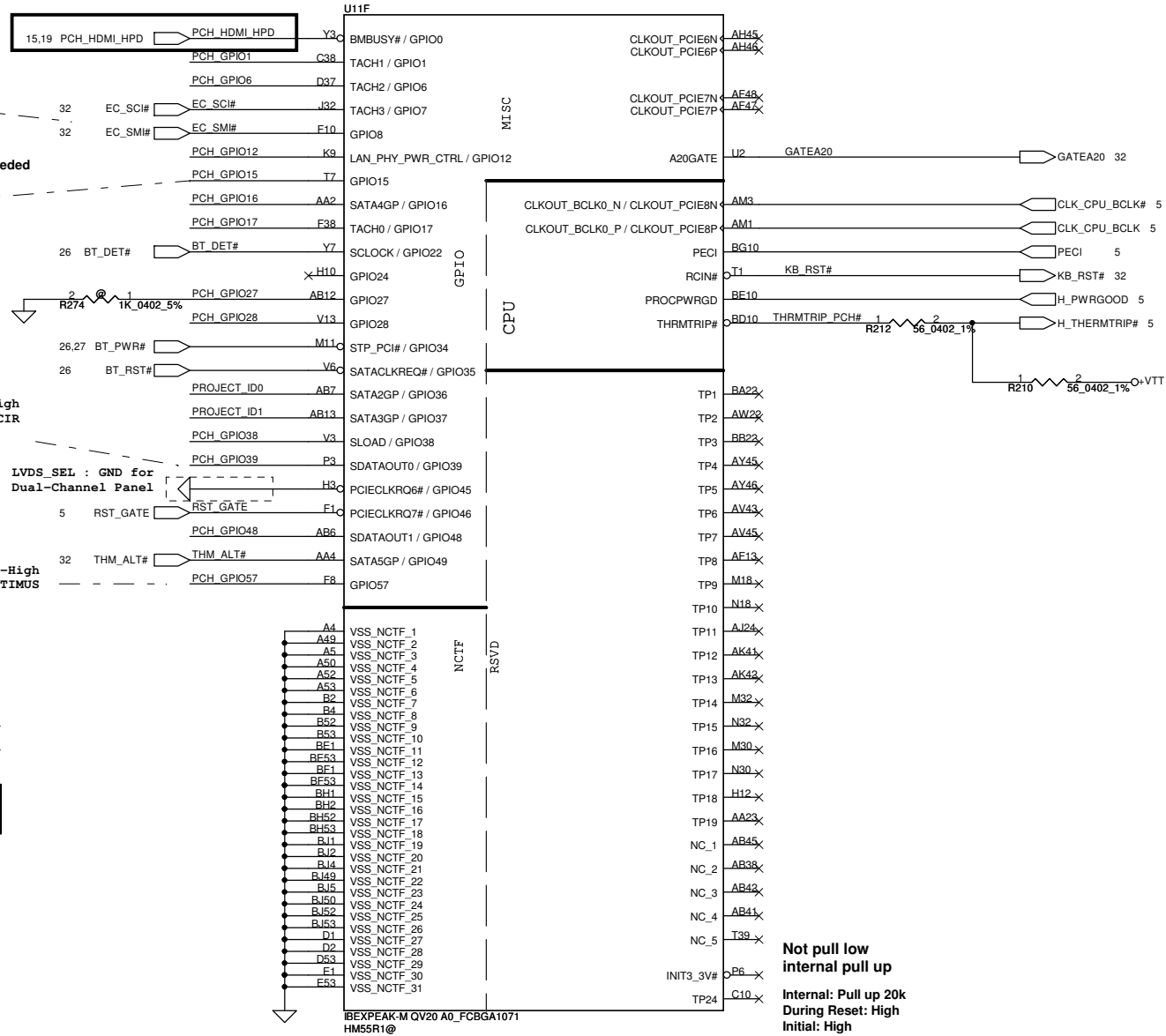
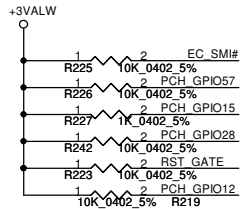
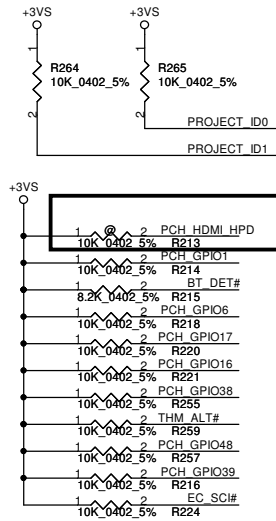
PCH_GPIO27 High = Enabled (Default)
Low = Disabled

GPIO39:
CIR_EN# : Pull-High
for non-support CIR

LVDS_SEL : GND for
Dual-Channel Panel

GPIO57:
OPTIMUS_EN# : Pull-High
for non-support OPTIMUS

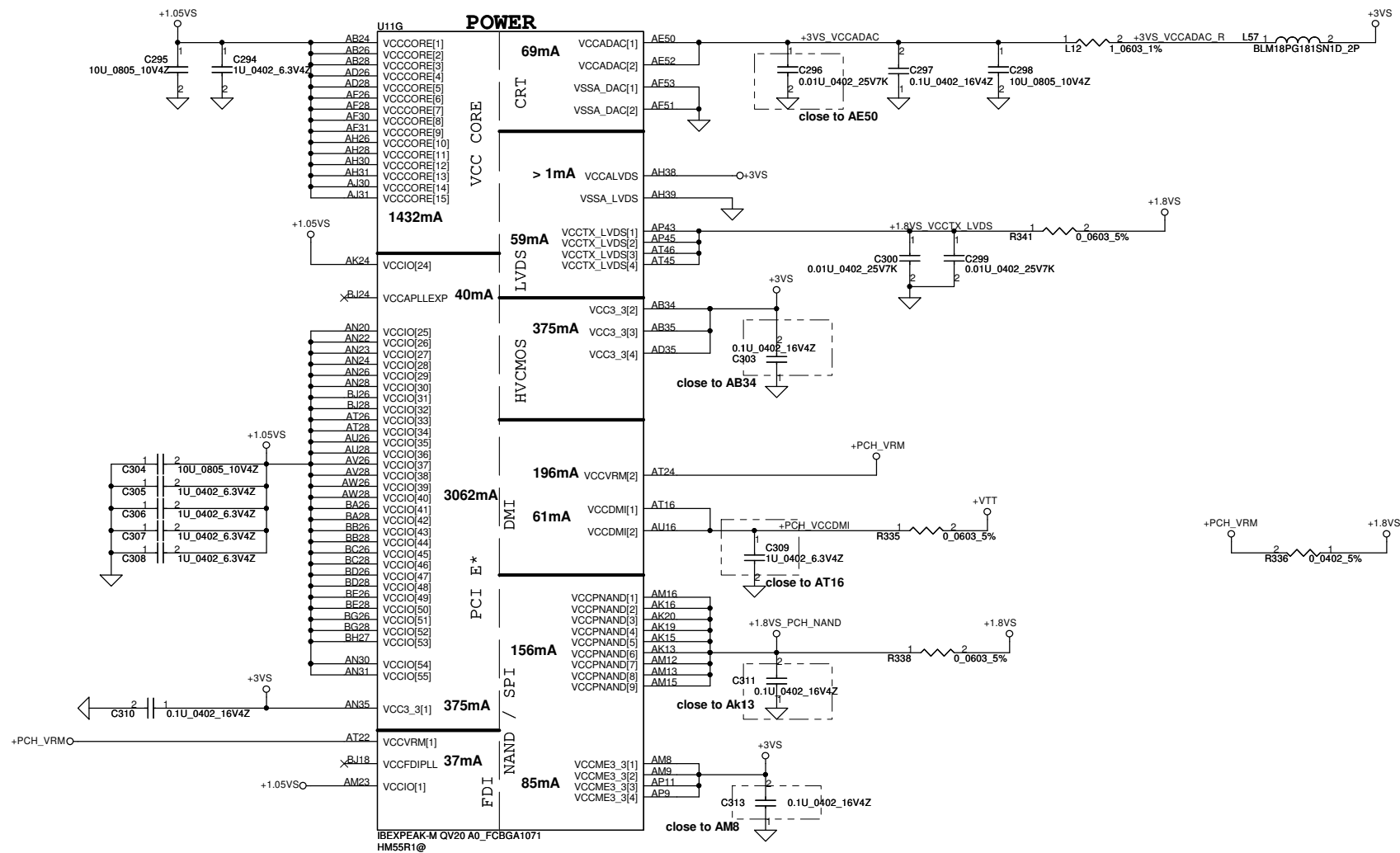
PROJECT_ID			
Name	ID0	ID1	
NBQAA 11.6/13.3"	L	L	
NBQAA 14"	L	H	
NWQAA 16"	H	L	
*NALAA 17.3"	H	H	



Not pull low
internal pull up

Internal: Pull up 20k
During Reset: High
Initial: High

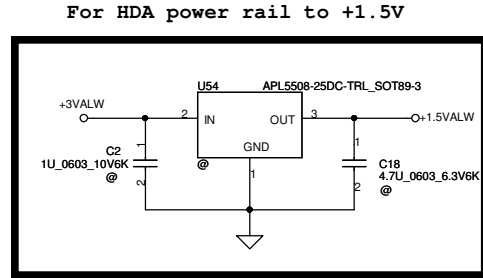
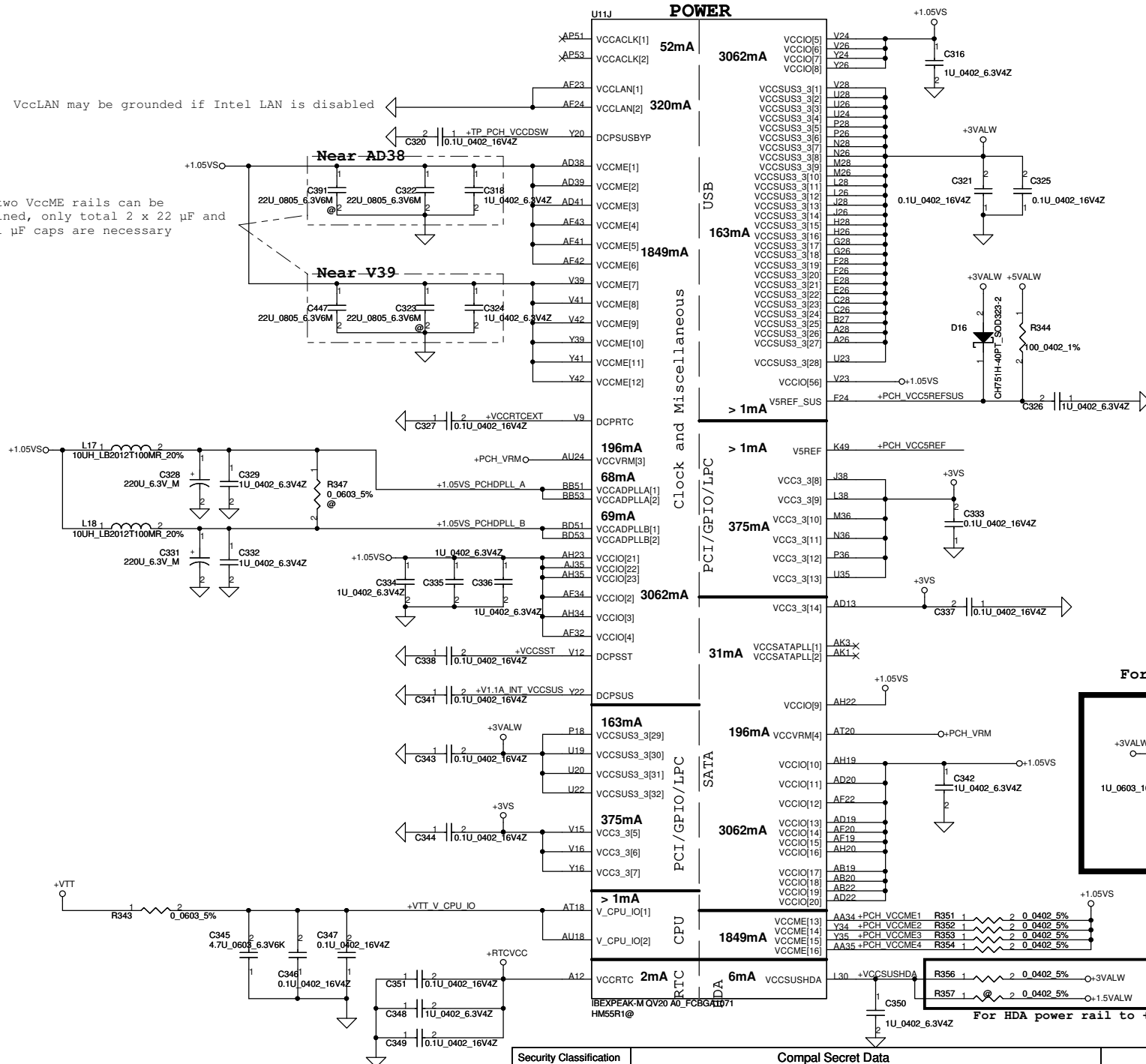
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	PCH CPU/GPIO
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				NALAA LA-6041P M/B	
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				Rev	1.0



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				NALAA LA-6041P M/B	
				Date:	Rev 1.0
				Tuesday, April 13, 2010	Sheet 22 of 48

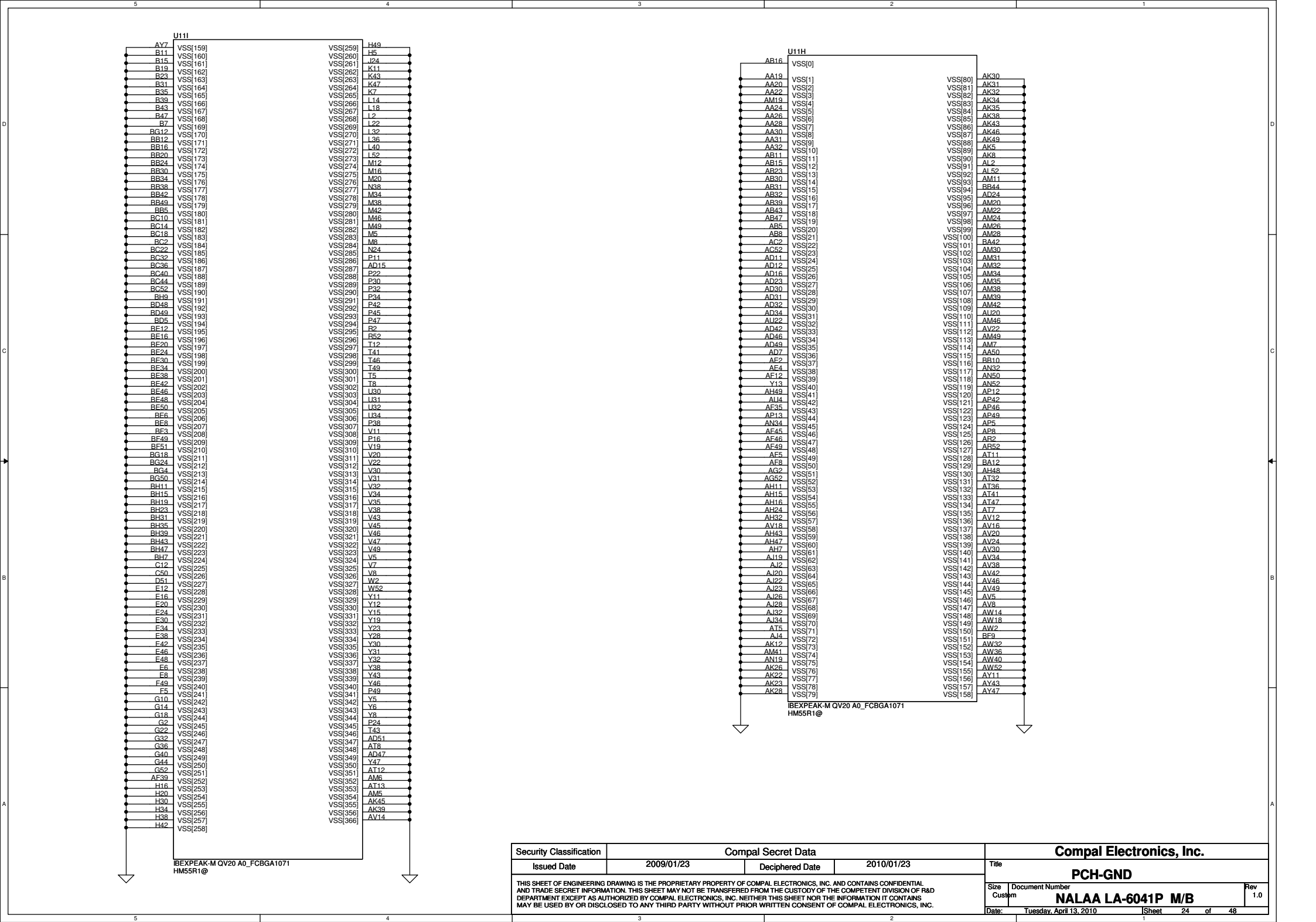
VccLAN may be grounded if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22 μ F and 2 x 1 μ F caps are necessary



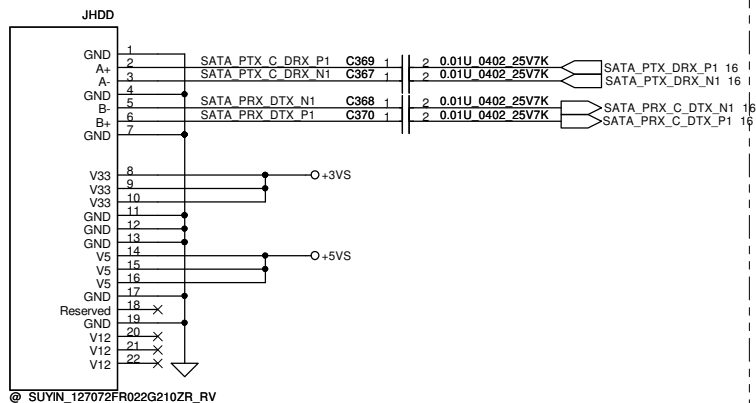
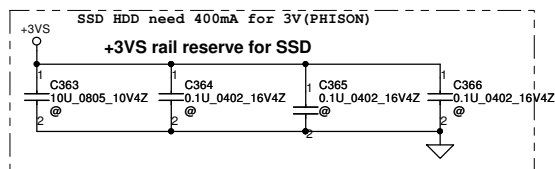
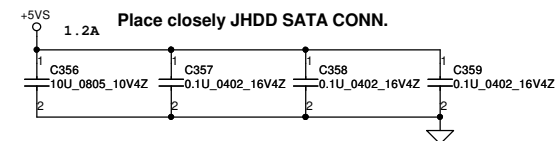
VCCSUS3HDA can be either 1.5V or 3.3V
For HDA power rail to +3.3V(default) / +1.5V

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Size	Custom	Document Number	NALAA LA-6041P M/B		Rev
Date:	Tuesday, April 13, 2010	Sheet	23	of	48

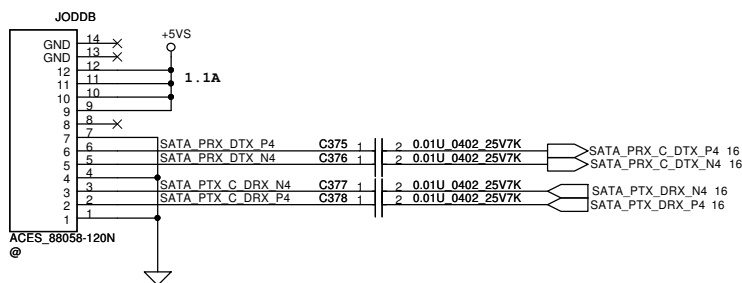


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Size	Document Number	Rev		1.0	
Custom	NALAA LA-6041P M/B				
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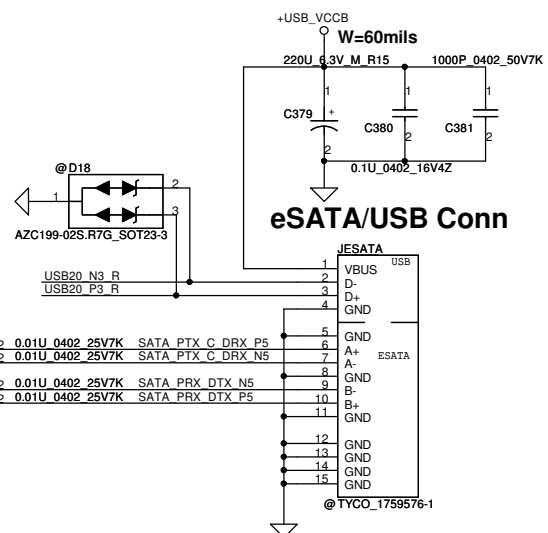
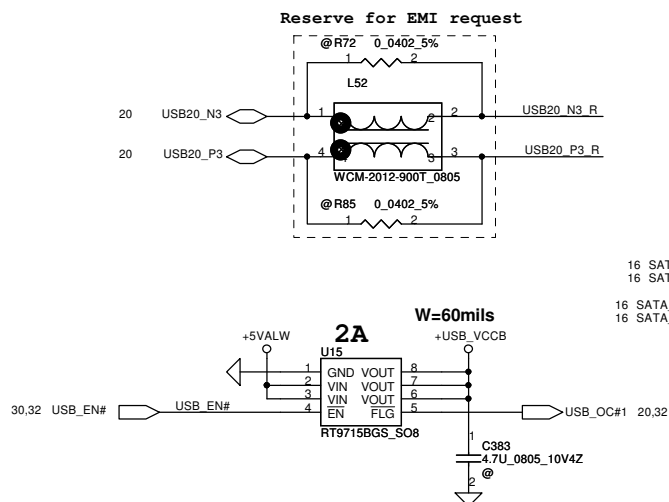
SATA HDD Conn.



SATA ODD Conn

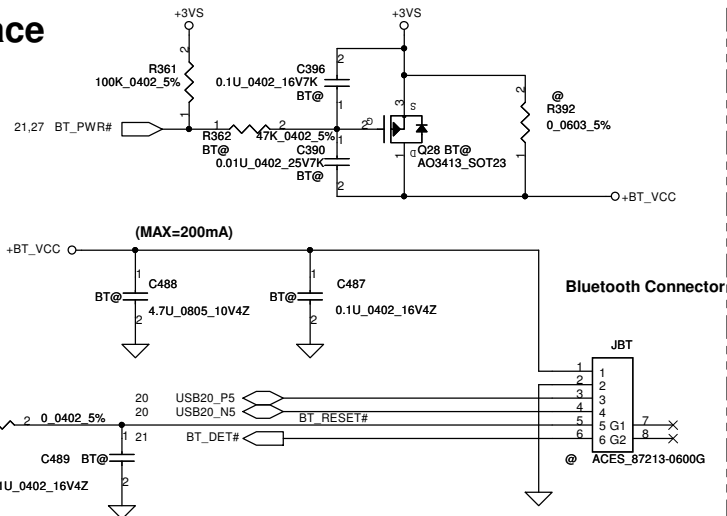


eSATA/USB

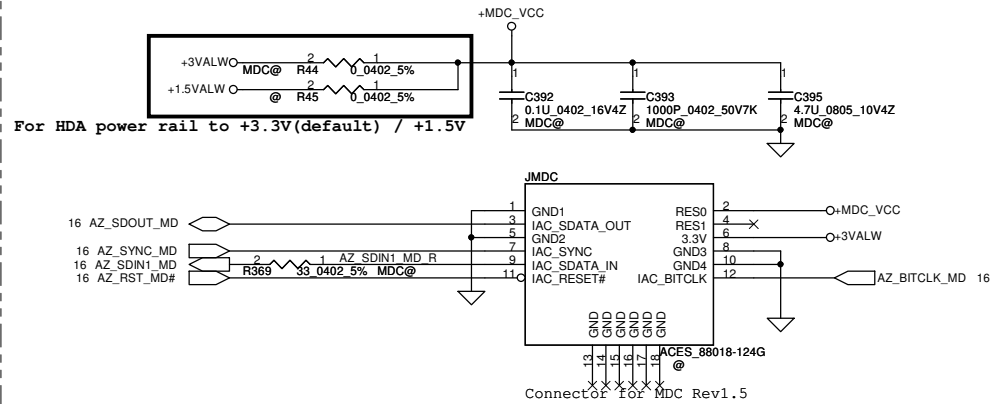


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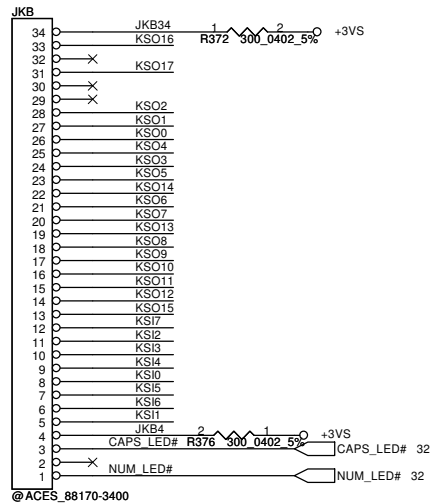
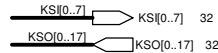
Bluetooth Interface



MDC 1.5 Conn.



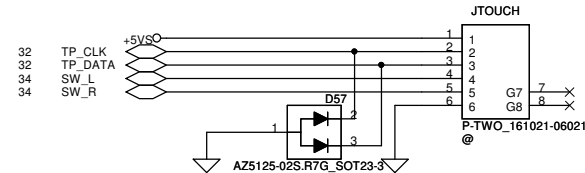
KEYBOARD
CONN. for 17"



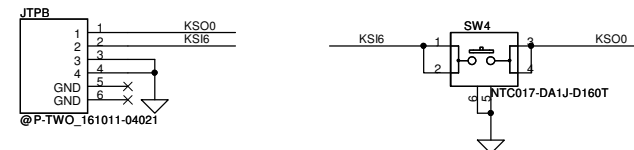
please close to JKB1

KSO16	1	2
KSO17	C401	100P_0402_50VBJ
KSO2	C402	100P_0402_50VBJ
KSO1	C401	100P_0402_50VBJ
KSO0	C405	100P_0402_50VBJ
KSO4	C406	100P_0402_50VBJ
KSO3	C407	100P_0402_50VBJ
KSO5	C408	100P_0402_50VBJ
KSO14	C409	100P_0402_50VBJ
KSO6	C410	100P_0402_50VBJ
KSO7	C411	100P_0402_50VBJ
KSO13	C412	100P_0402_50VBJ
KSO8	C413	100P_0402_50VBJ
KSO9	C415	100P_0402_50VBJ
KSO10	C416	100P_0402_50VBJ
KSO11	C417	100P_0402_50VBJ
KSO12	C418	100P_0402_50VBJ
KSO15	C419	100P_0402_50VBJ
KSI7	C420	100P_0402_50VBJ
KSI2	C421	100P_0402_50VBJ
KSI3	C422	100P_0402_50VBJ
KSI4	C423	100P_0402_50VBJ
KSI0	C424	100P_0402_50VBJ
KSI5	C425	100P_0402_50VBJ
KSI6	C427	100P_0402_50VBJ
KSI1	C429	100P_0402_50VBJ
CAPS LED#	C431	100P_0402_50VBJ
NUM LED#	C433	100P_0402_50VBJ
	C435	100P_0402_50VBJ

Touch PAD Connector

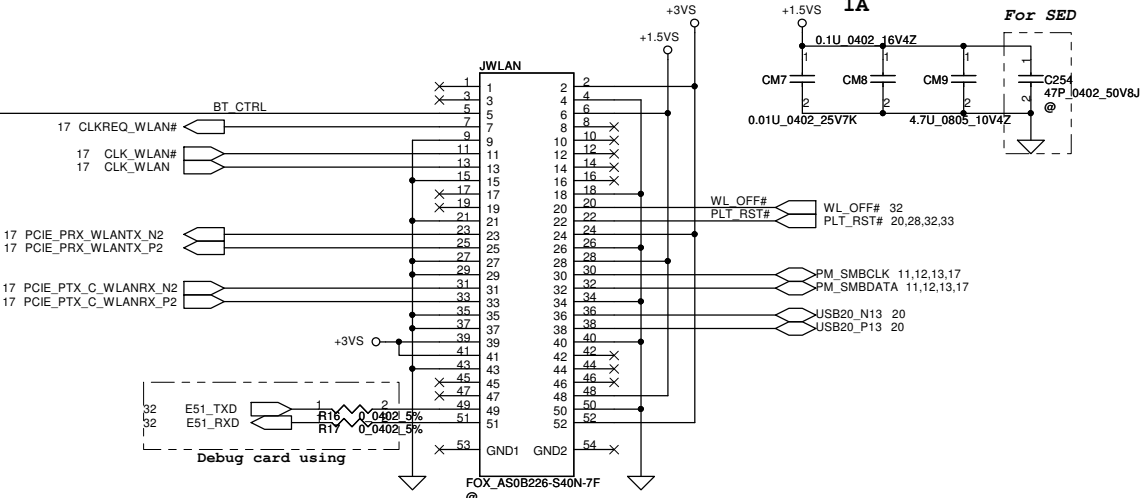
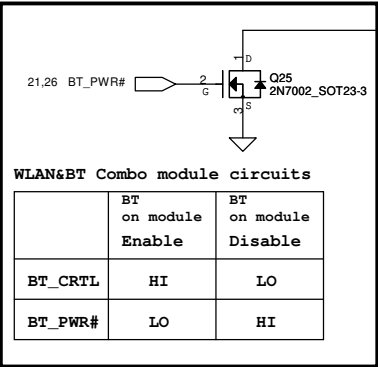


Touch ON OFF/B Connector

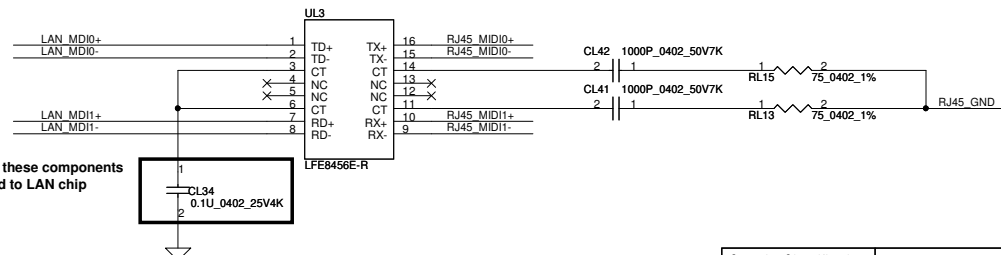
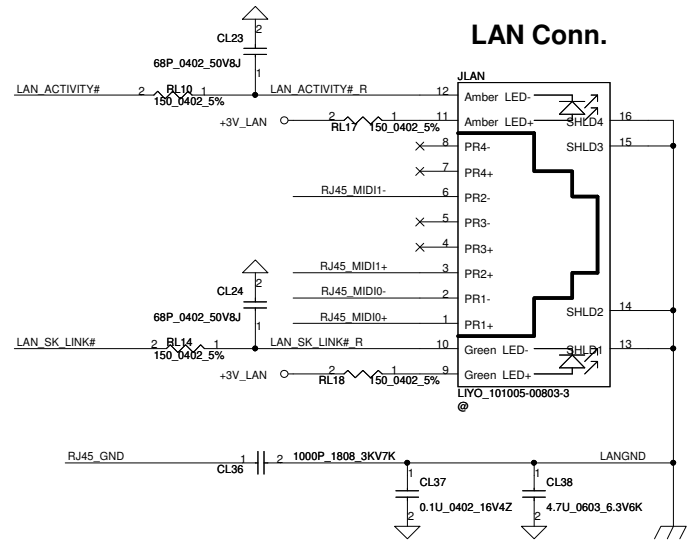
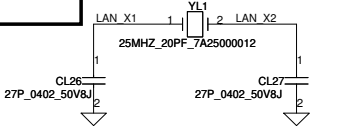
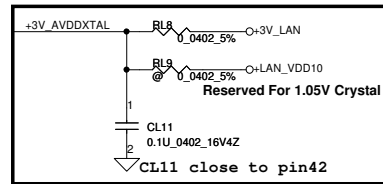
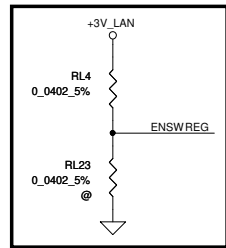
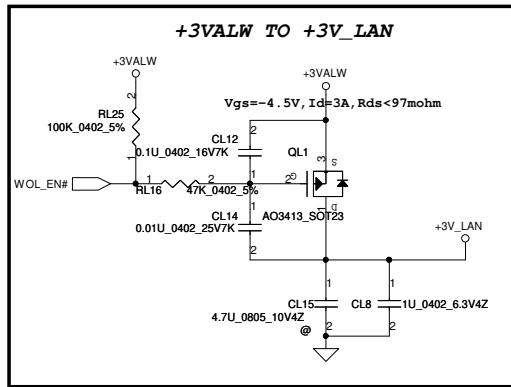
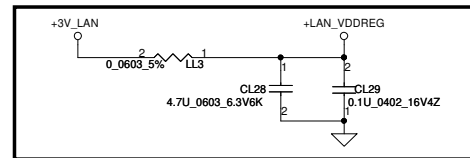
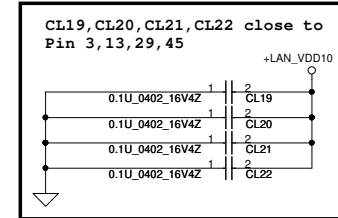
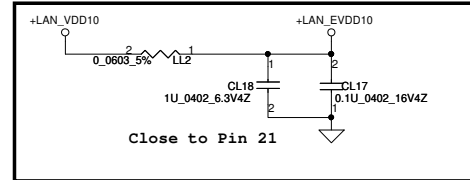
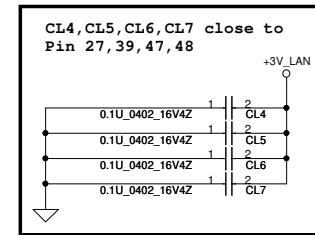
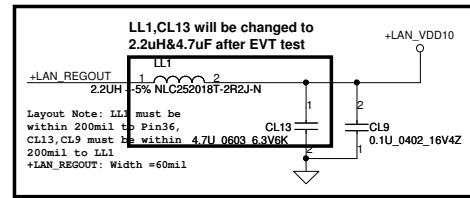
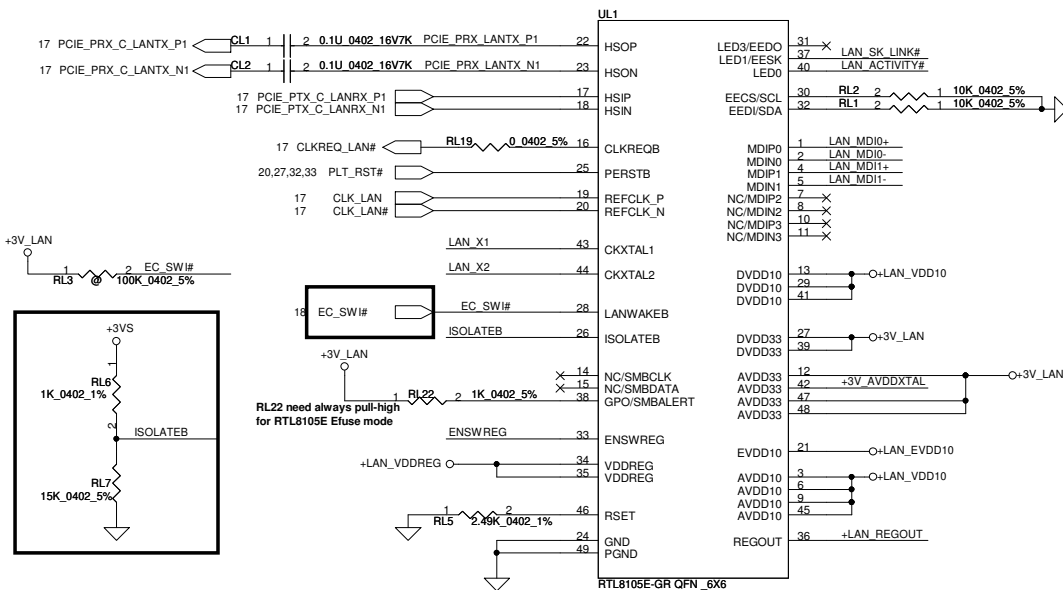


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					NALAA LA-6041P M/B	1.0
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PCle Mini Card-WLAN/WiMax

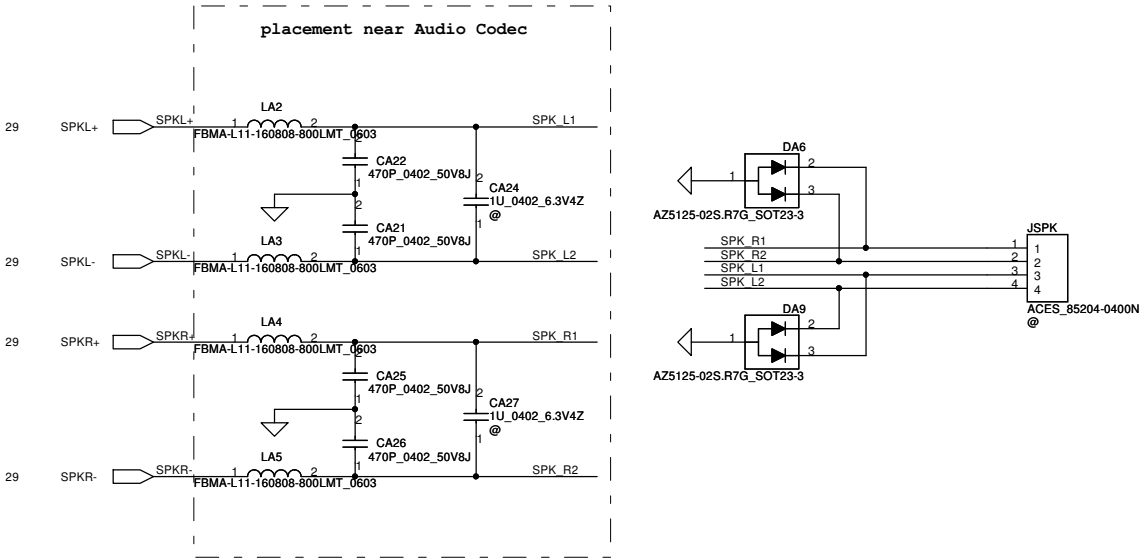


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Size		Document Number			Rev
		NALAA LA-6041P M/B			1.0
Date:		Tuesday, April 13, 2010		Sheet	27 of 48

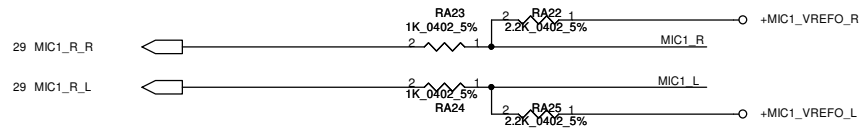


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Deciphered Date				2010/01/23				NALAA-6041P M/B			
Title				Date				Tuesday, April 13, 2010			
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Document Number				Rev				1.0			
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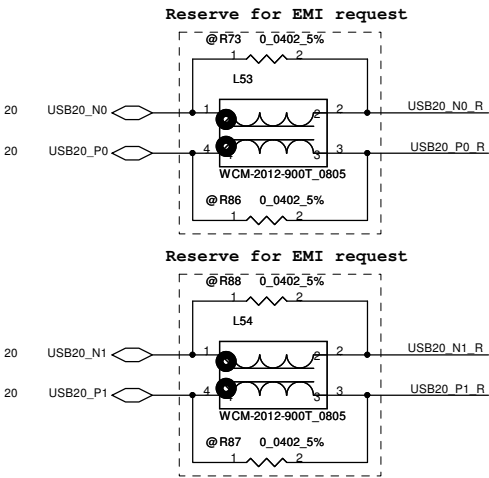
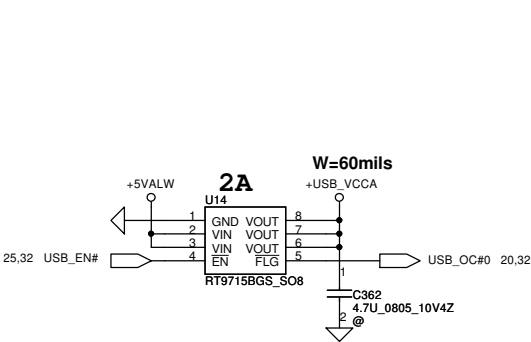
Speaker Connector



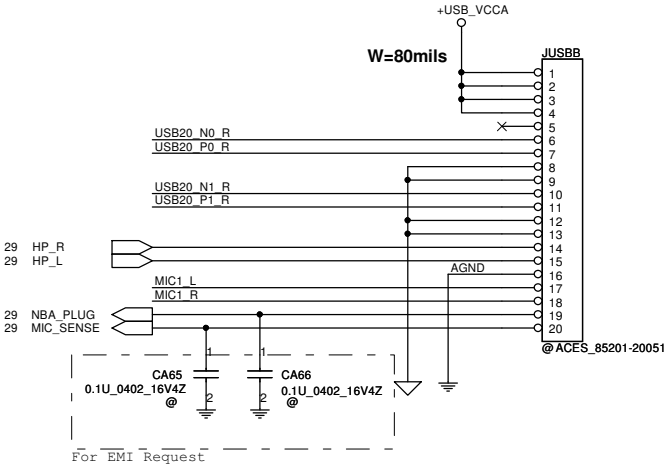
Ext.MIC/LINE IN



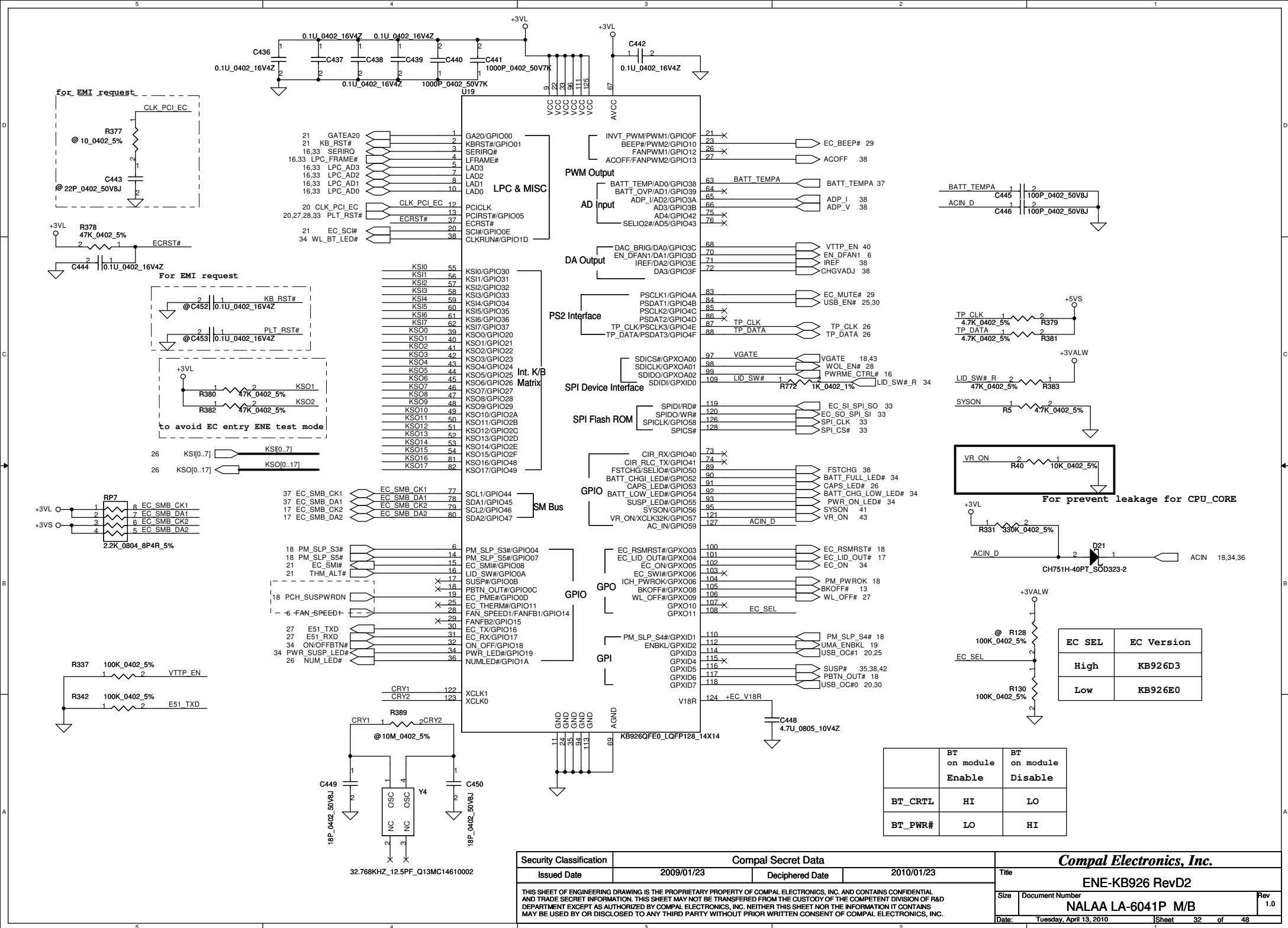
USB Board



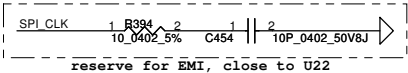
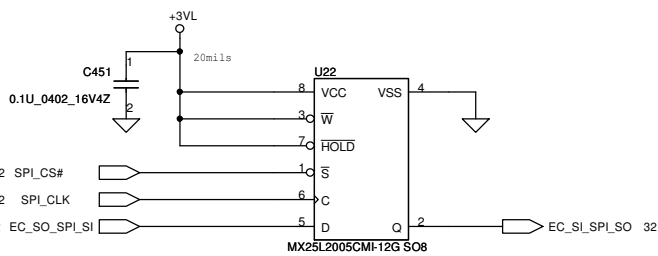
Audio & USB Sub-Board Conn.



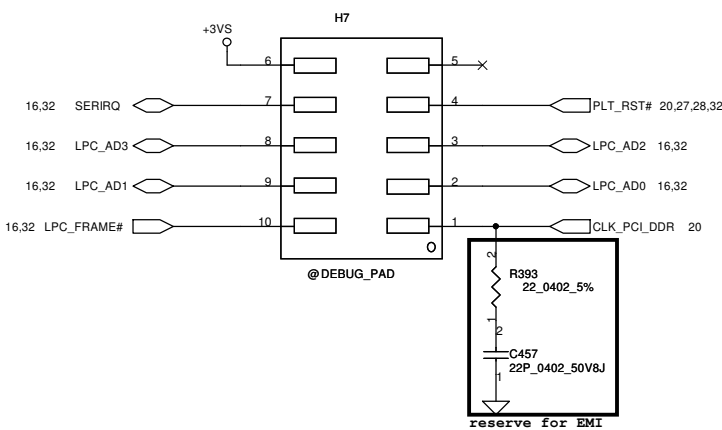
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SPI Flash (256KB)
Socket: SP07000F500 & SP07000H900

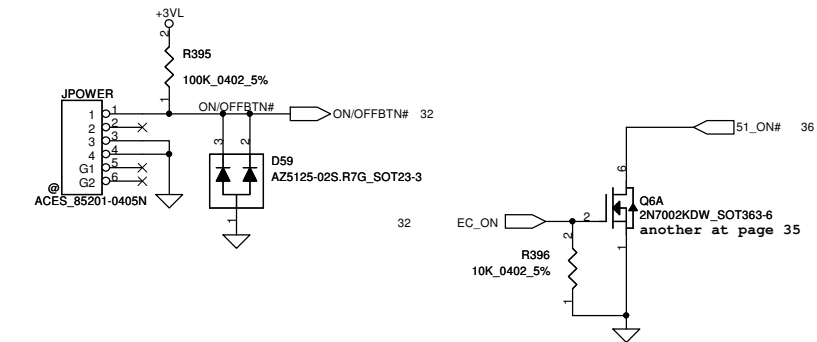


LPC Debug Port
Please place the PAD under DDR DIMM.

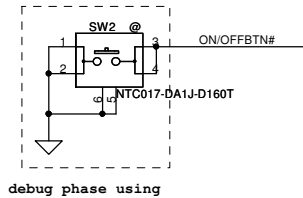


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				Size	Document Number	Rev
					NALAA LA-6041P M/B	1.0
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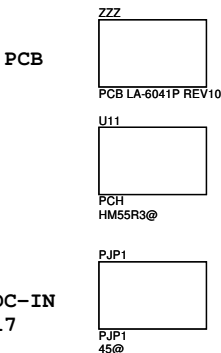
Power Button



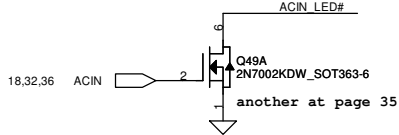
Debug Button



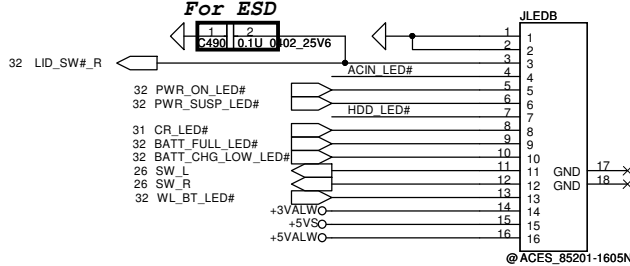
ISPD



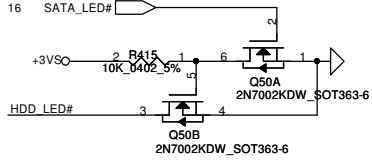
DC-IN LED Control Circuit



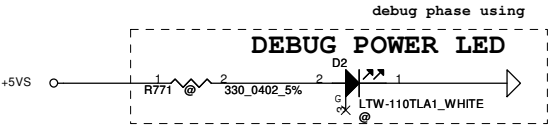
LED/B Conn.



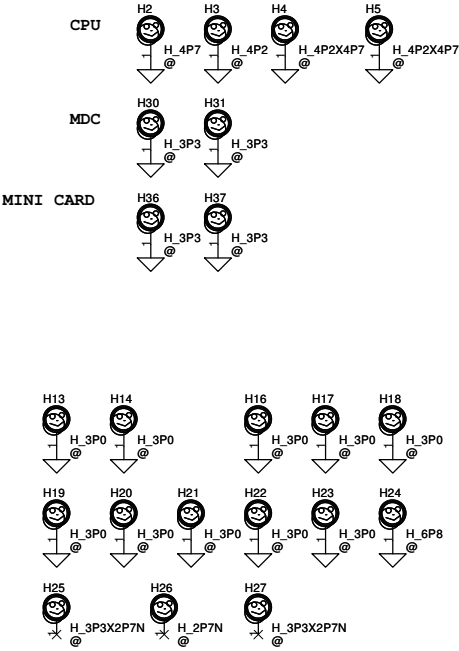
HDD LED Control Circuit



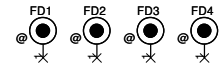
POWER LED Control Circuit



Screw Hole

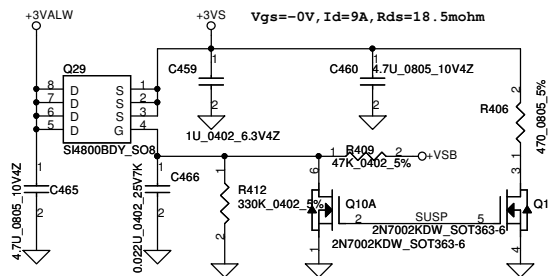


PCB Fedical Mark PAD

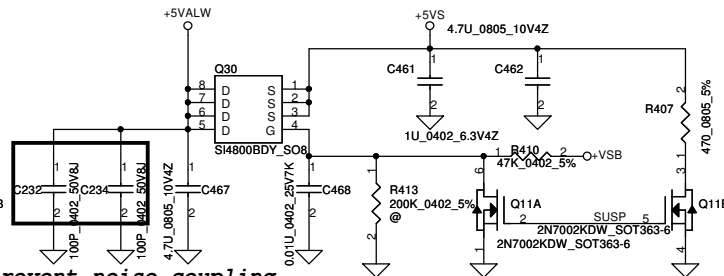


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				Date:	Tuesday, April 13, 2010
				Sheet	34 of 48

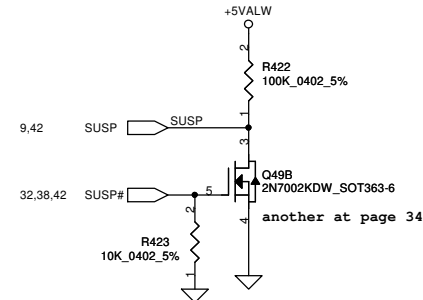
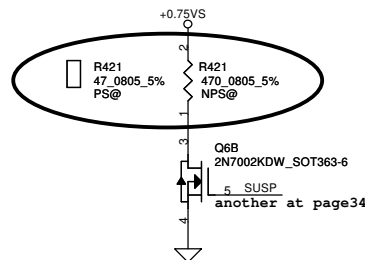
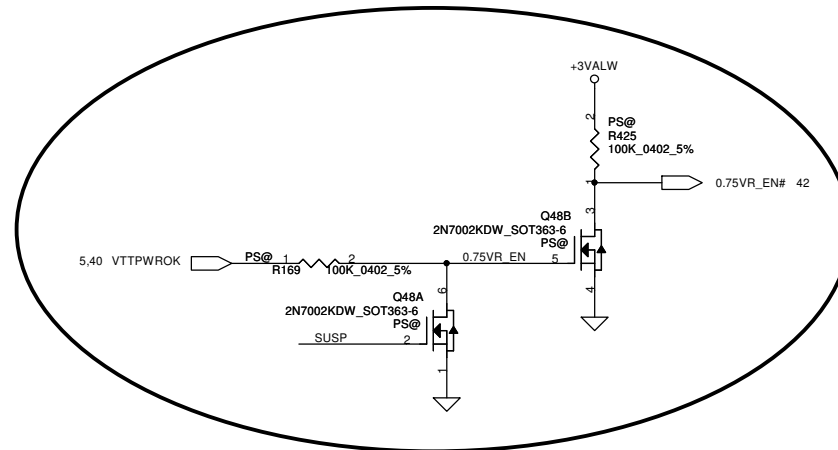
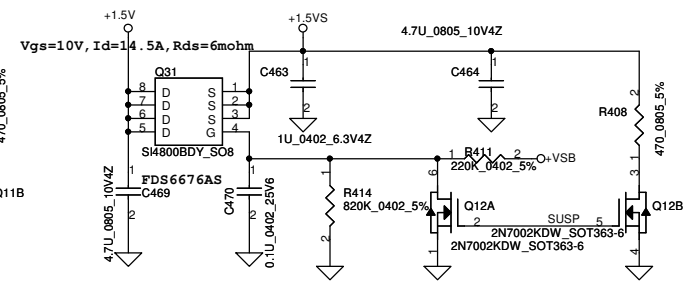
+3VALW TO +3VS



+5VALW TO +5VS

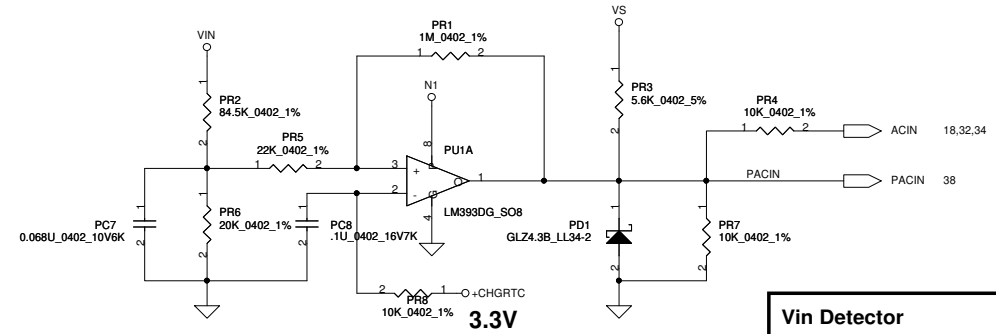
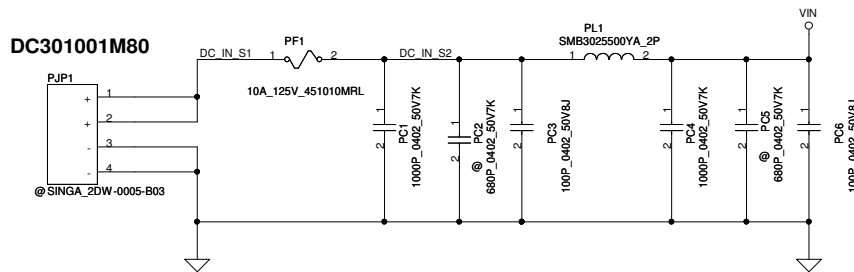


+1.5V to +1.5VS



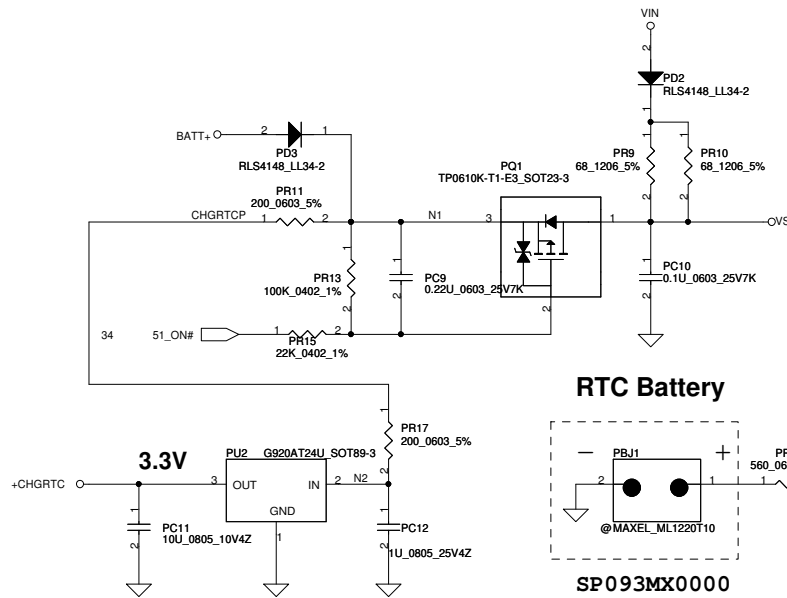
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DC301001M80

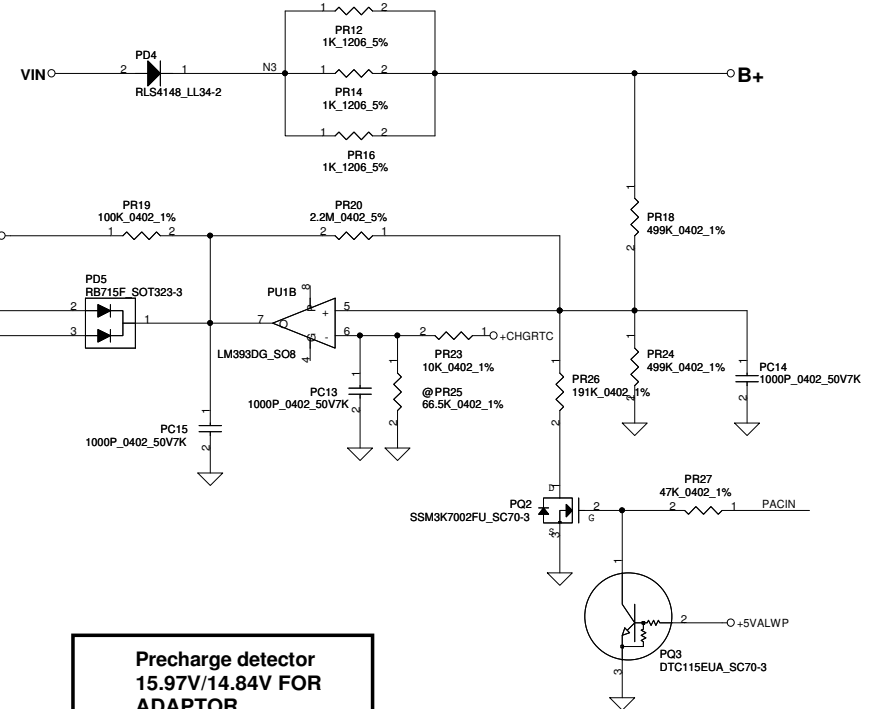
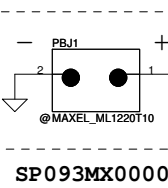


Vin Detector

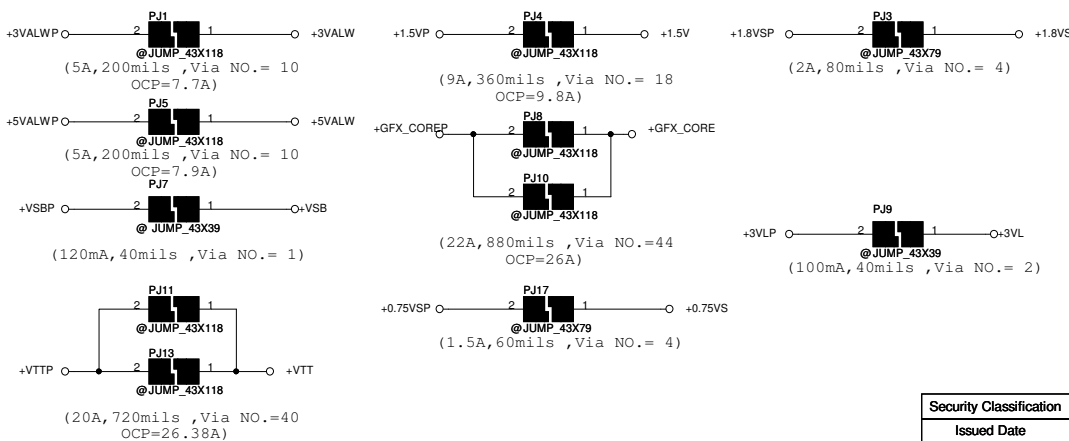
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



RTC Battery



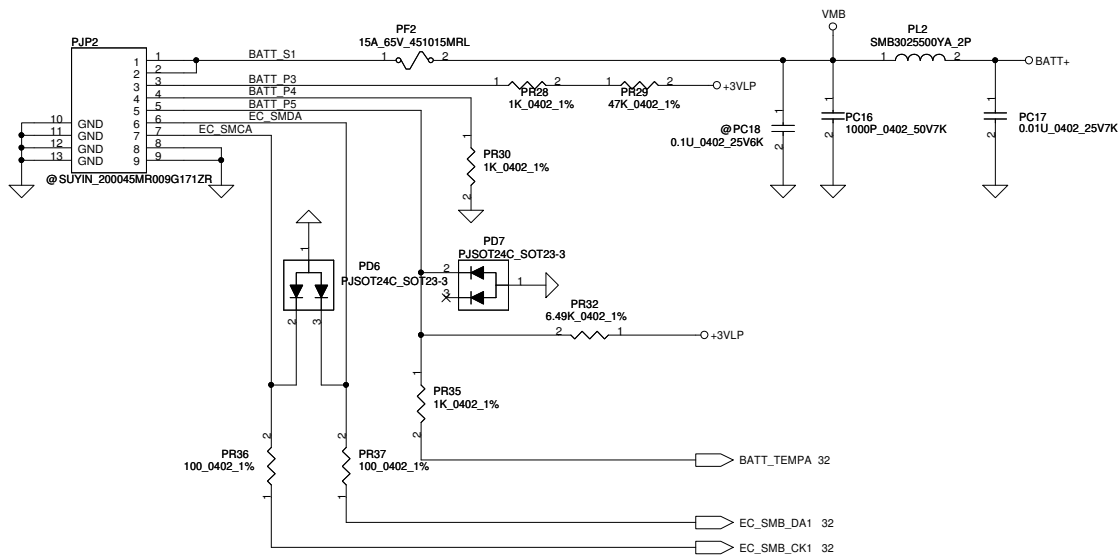
Precharge detector 15.97V/14.84V FOR ADAPTOR



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				Deciphered Date				DCIN / DETECTOR			
				2010/01/23				Size			
								Document Number			
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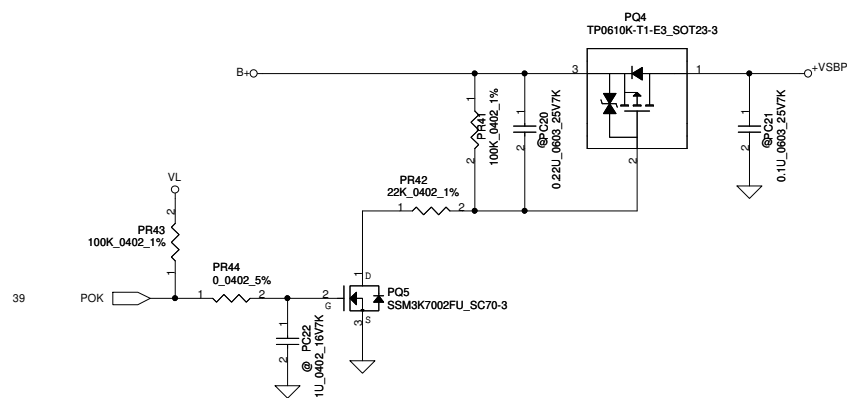
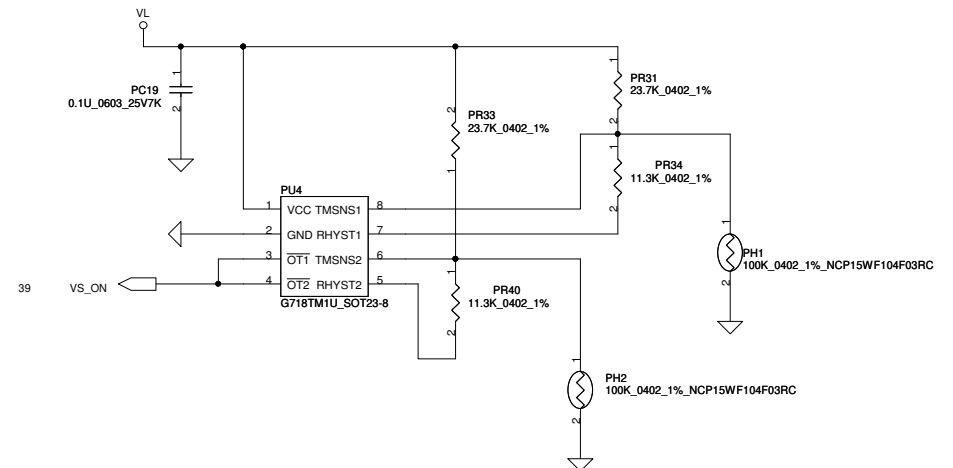


PH1 under CPU botten side :

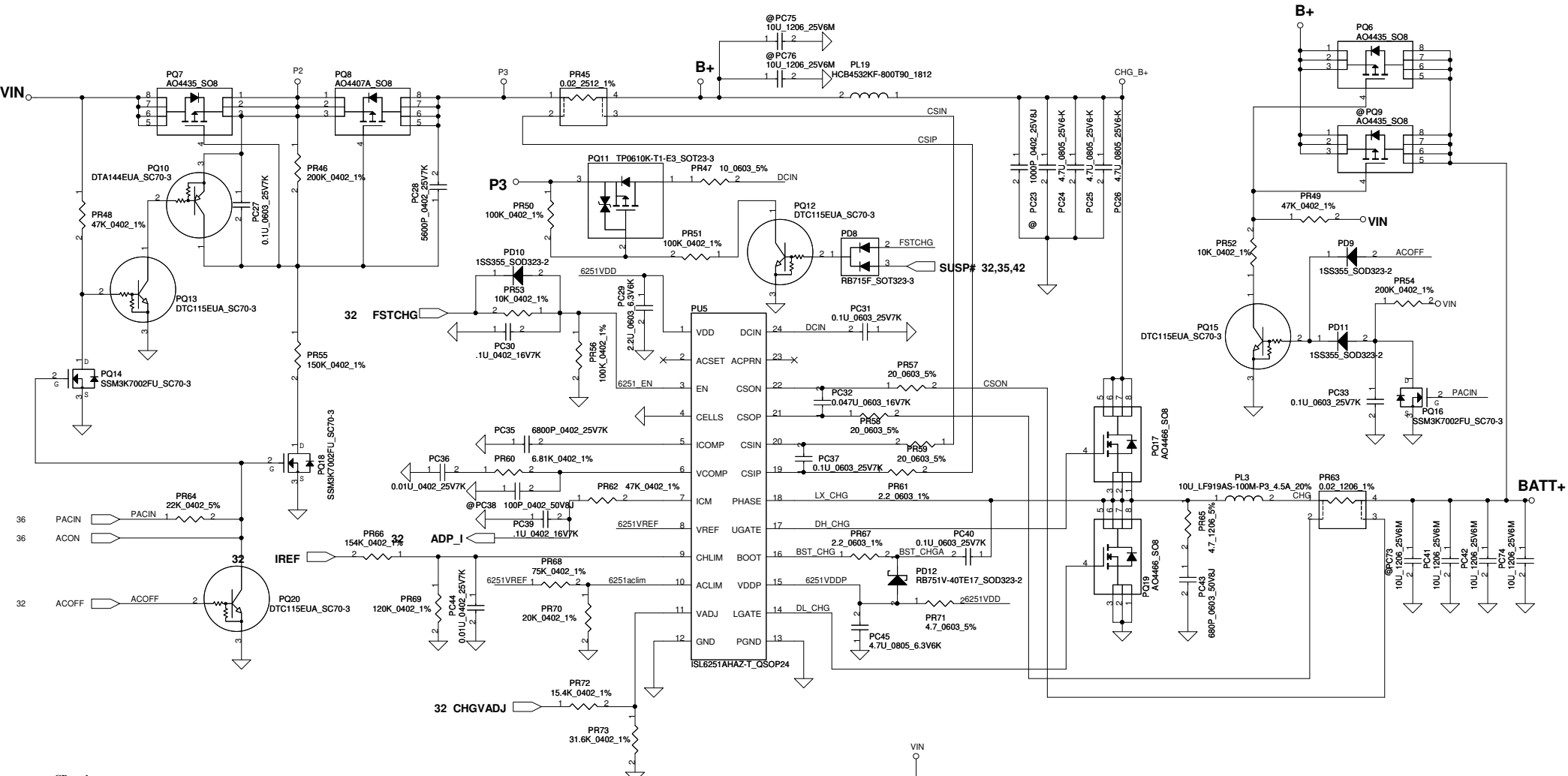
CPU thermal protection at 90 degree C
Recovery at 56 degree C

PH2 near main Battery CONN :

BAT. thermal protection at 90 degree C
Recovery at 56 degree C



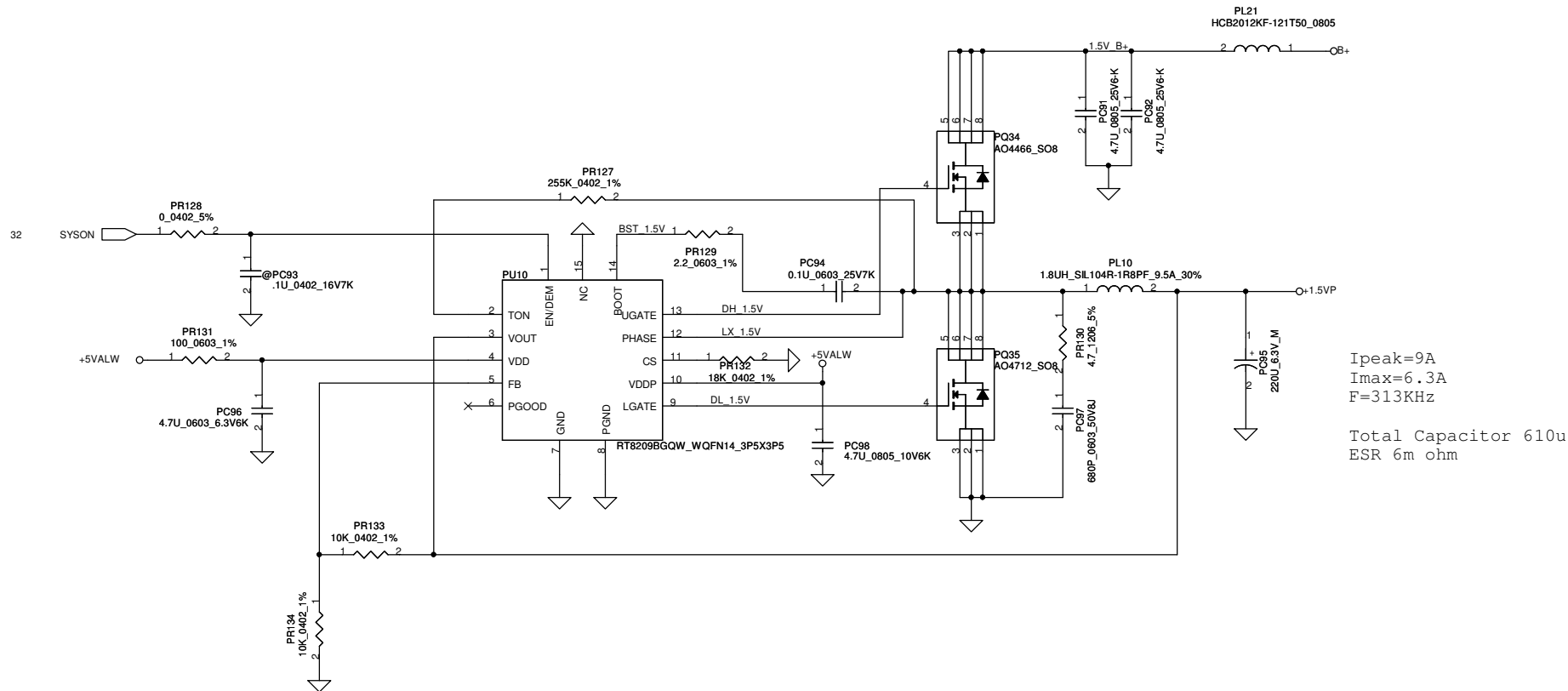
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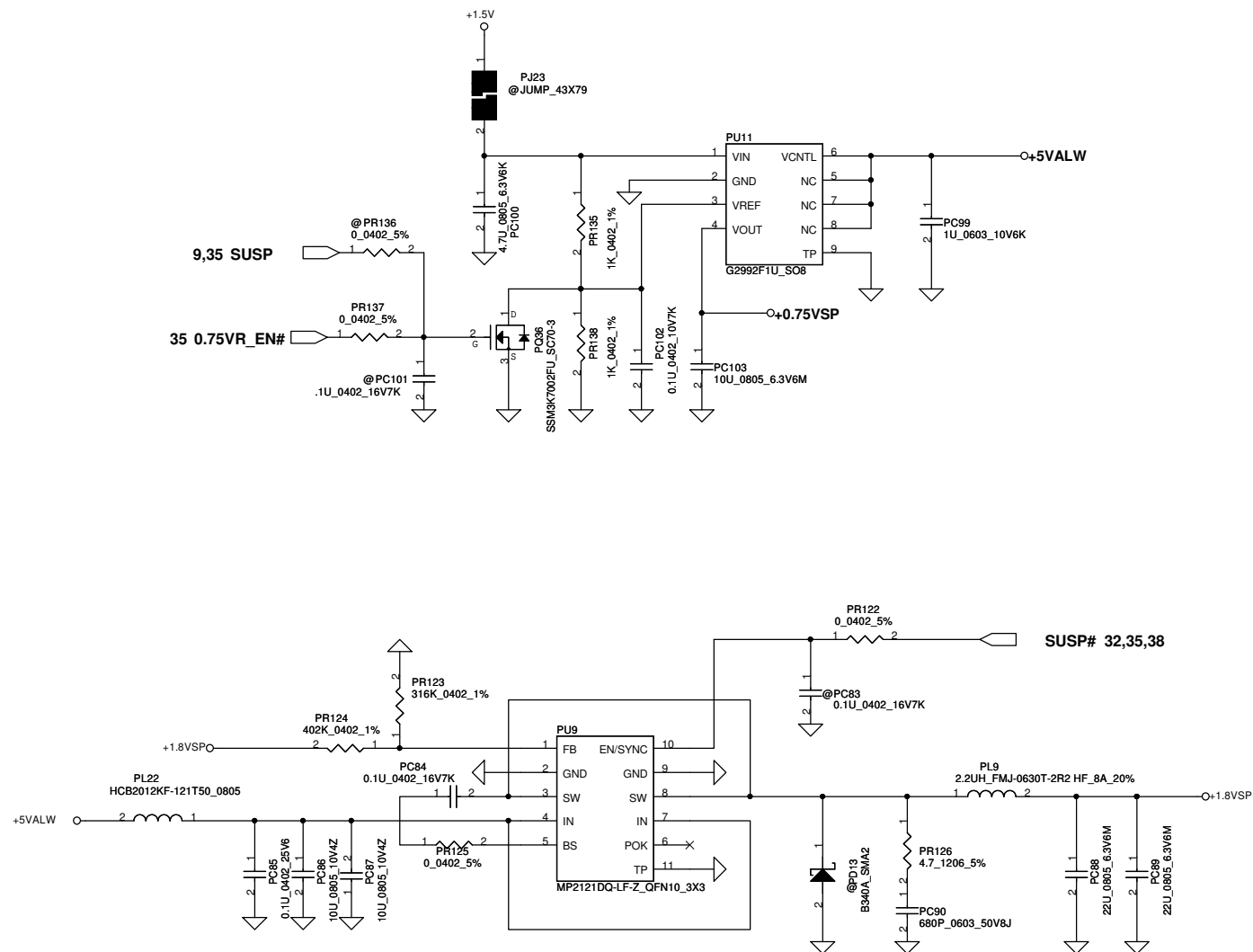
CP mode
 $I_{ada} = 0 \sim 3.42A (65W)$ $CP = 92\% \cdot I_{ada}$; $CP = 3.147A$
 $V_{acim} = 1.08V (65W)$ $PR68 = 75k$ $PR45 = 0.02$

$CC = 0.25A \sim 3A$
 $I_{REF} = 1.016 \cdot I_{charge}$
 $I_{REF} = 0.254V \sim 3.048V$
 V_{CHLIM} need over 95mV

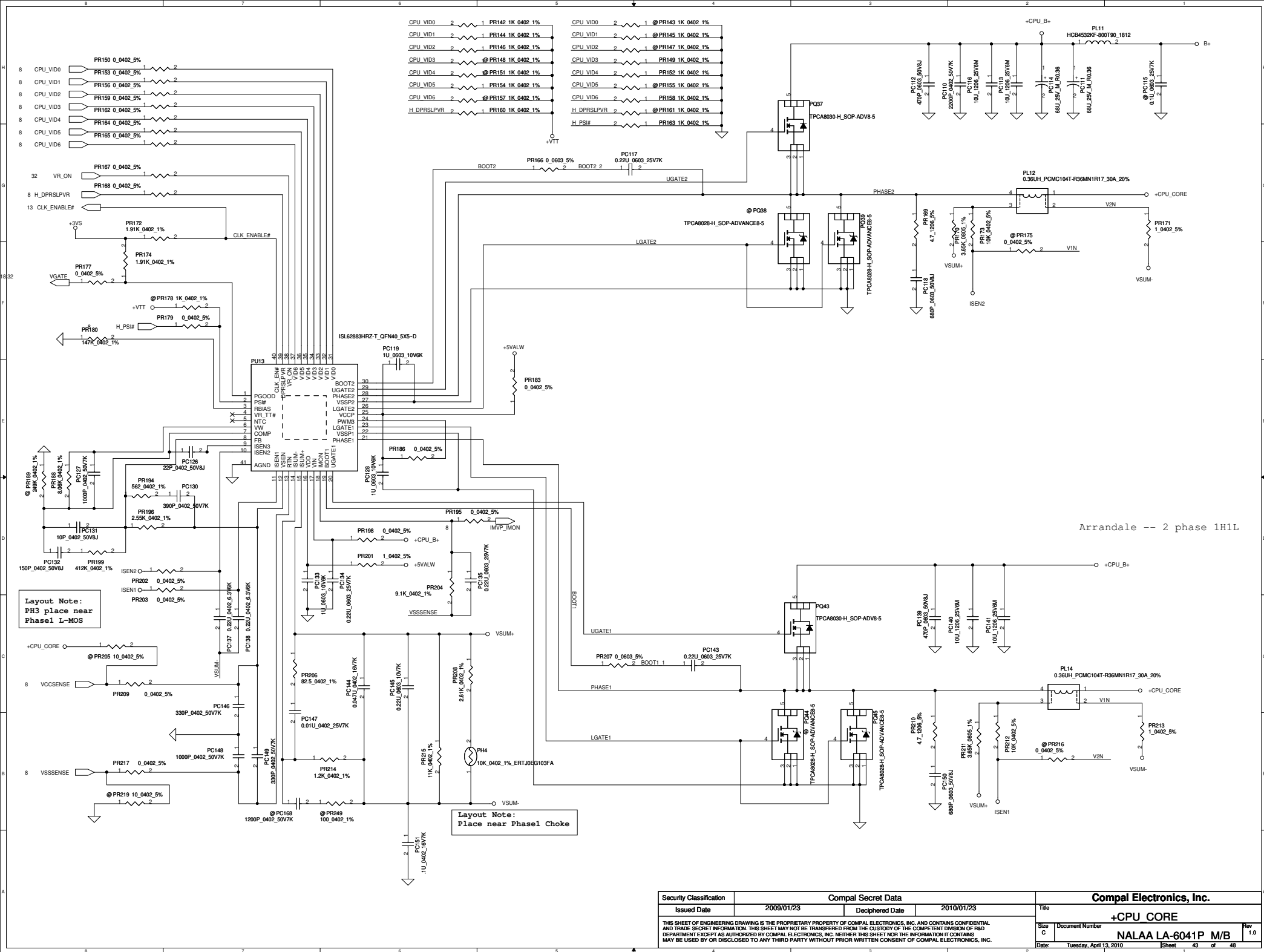
CHGVADJ = (Vcell - 4) / 0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V



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PIR (Product Improve Record)

NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
11/26	34		Change C296,C299,C300,CA64,CM1,CM7 from SE072103280 to SE068103K80	For reduce BOM type
12/09	34		Connect JLEDB.15&16 to GND	For T/P SW issue
12/09	25,30		Change U14 & U15 from SA00002XX00 to SA000033H00	For material issue
12/16	15		Change R159 from IHDMI@ to @	For HDMI level shift disable function
12/16	31		Change CC2 from CARD@ to @	For Card Reader issue
12/16	34		Modify JLEDB pin define	For customer concern
12/16	21		Del R222 and connect PCH GPIO45 to GND	For LVDS_SEL (Dual-Channel)
12/16	13		Change U5 from SA00003HQ00 to SA00003HQ10	For CLK GEN update
12/16	27		Add R22 and Net BT_PWR#_R to connect JWLAN Pin5	For BT/WLAN combo Mini Card
12/16	16		Change U13 footprint to M25P80-VMW6TP_SO8 and delete BOM structure.	For delete ROM socket
12/16	34		Change H36, H37 from H_3P3 to H_3P8.	For ME modify
12/16	26		Reverse JBT pin definition	For ME modify
12/16	31		Change CC2 from 0.1u to 100P (SE071101J80) and add BOM structure @.	For Card Reader issue
12/16	34		Change JPOWER footprint to ACES_85201-0405N_4P.	For ME modify
12/16	26		Change JTPB footprint to P-TWO_161011-04021_4P-T.	For ME modify
12/16	34		Change JLEDB footprint to ACES_85201-1605N_16P	For ME modify
12/16	30		Change JUSBB footprint to ACES_85201-20051_20P	For ME modify
12/16	34		Del H15	For ME modify
12/21	34		Change H36,H37 from H_3P8 to H_3P3	For ME modify
12/21	13		Change +LCD_INV from JLVDS.35 to JLVDS.40	For prevent burn issue
12/21	13		Change BKOFF#_R from JLVDS.40 to JLVDS.35	For prevent burn issue
12/23	16,32		Change net name from PWRME_CTRL to PWRME_CTRL#	For signal is LOW active
12/23	08		Add C125 SF000002Y00	For co-lay with C123
12/23	09		Del C128	For del co-lay with C185
12/23	09		Del C140	For del co-lay with C217
12/23	17		Change Y2 P/N from SJ125P0M200 to SJ100003300	For cost down plan
12/23	27		Delete R22 and BT_PWR#_R and add Q25 and BT_CTRL at JWLAN pin5	For BT/WLAN combo Mini Card
12/24	29		Change RA26 to L56 bead 300 ohm FBMA-L10-160808-301LMT(SM010017710)	For EMI issue
12/24	15		Add R96 1K ohm to connect HDMI_HPD and U9.1	For prevent U9 ESD damage issue
12/24	30		Change LA2,LA3,LA4,LA5 to 80 Ohm bead FBMA-L11-160808-800LMT (SM010015410)	For EMI request
12/24	30		Change CA21,CA22,CA25,CA26 to 470P (SE071471J80)	For EMI request
12/24	26		Del R361 BOM structure BT@ (always mount)	For BT function
12/28	26		Change R392 BOM structure from BT@ to @.	For BT function
12/28	26		Change C159,C160,C185,C217,C268 footprint from C_PXC6P3VC220MF60 to C_MP2VU390MC5R7.	
12/28	25		Change JODDB footprint to ACES_88058-120N_12P-T.	For DFX request
12/29	13		Del C292	Only for NSWAA
12/29	28		Change UL3 P/N from SP050005W00 to SP050005V00	For EMI request
12/29	28		Change UL1 P/N from SA00003PO00 to SA00003PO10	For IC chip revise version
01/05	06		Change C4 from SE068102J80 to SE074102K80	For component common design

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NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01/19	13		Change BKOFF#_R from JLVDS.35 to JLVDS.33	For prevent burn issue
01/27	32		Add pull down R40 10Kohm at VR_ON.	For prevent leakage for CPU_CORE
01/27	25		Change D18 from SCA00000A00 to SC600001600	For ESD request
01/27	13,26,30,34		Change D57,D58,D59,DA6,DA9 from SCA00000G00 to SCA00001A00	For ESD request
01/27	15		Add pull down R148 2.2Kohm at HDMI_TXC-.	For UMA HDMI level shift display compatibility issue
01/27	28		Change UL3 from SP050005W00 to SP050005V00	For ESD request
01/27	29		Change UA1 from SA00003QR00 to SA00003QR10	For Realtek update
01/27	32		Change R128 BOM structure from mount to un-mount.	For EC update
01/27	32		Change R130 BOM structure from un-mount to mount.	For EC update
01/27	32		Change U19 from SA00001J580 to SA00001J5A0.	For EC update
02/01	30		Change JSPK pin define	For common SPK material
02/01	16		Add D19 & R133 between +RTCVCC and RTCVREF.	For prevent RTC empty then can not boot up issue
02/01	19		Change R77 from SD028100280 to SD028100380	For INTEL issue (pending interrupts from the PCH for unused HDMI ports)
02/01	05		Add C225	For prevent noise issue
02/04	22		Change L12 from SM010028480 to SHI00002K00	For CRT wave issue
02/04	28		Change LL1 from SHI00004T00 to SHI0000AA00	For package limitation, Realtek criteria, 2ND source reason
02/04	28		Change CL13 from SE000000I10 to SE107475K80	For package limitation, Realtek criteria, 2ND source reason

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NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
02/23	15		Change R167 BOM structure from @ to IHDMI@.	For reduce HDMI choke plan
02/23	15		Change R163 BOM structure from IHDMI@ to @.	For reduce HDMI choke plan
02/23	15		Change R160 from SD028330180 (3.3K ohm) to SD034390180 (3.9K ohm).	For reduce HDMI choke plan
02/23	15		Change L8,L9,L10,L11 BOM structure from IHDMI@ to @.	For reduce HDMI choke plan
02/23	15		Change R157,R173,R175,R180,R182,R183,R187,R188 BOM structure from @ to IHDMI@.	For reduce HDMI choke plan
02/23	22		Change L12 from SHI00002K00 (10UH +-20%) to SD008100B80 (1 ohm +-1% 0805).	For CRT wave issue
02/23	16		Delete D19 & R133	For prevent RTC empty then can not boot up issue
02/23	23		Change U54,C2,C18 BOM structure to @.	For reserve HDA power rail to +1.5V
02/23	26,34		Change SW2,SW4 from SN100000F00 to SN100002Y00 and add BOM structure @ at SW2.	For cost concern
03/09	29,32		Add Net EC_MUTE# from EC pin 83 to codec Pin4	For system has abnormally noise after S3 resume.
03/09	29		Add pull Low RA45 4.7K ohm.	For system has abnormally noise after S3 resume.
03/09	29		Change CA16 BOM structure to @.	For system has abnormally noise after S3 resume.
03/11	22		Add L57.	For prevent EMI and CRT wave issue.
03/11	25,30		Change U14,U15 from SA000033H00 to SA00002XX00.	For sourcer suggestion.
03/11	25,30		Change ZZZ from DA60000GC00 to DAZ0CK00100.	For Pre-MP phase.
03/11	06		Change U1 from SA00002XA00 to SA000035G00.	For voltage drop issue.
03/11	34		Change R771,D2 BOM structure to @.	For Pre-MP phase.
03/11	22		Add net name +3VS_VCCADAC_R	For net nameing rule
03/15	34		Add R772 & C490 and net name LID_SW#_R	For prevent ESD damage
03/15	22		Change L12 from SD008100B80 to SD014100B80.	For package size
03/16	29		Change CA12.1, RA12.2, CA18.2 connect to GNDA	For high frequency noise issue at S0
03/16	13		Add C231	For prevent noise coupling
03/17	35		Add C232,C234	For prevent noise coupling
03/17	31		Add CC9,CC10,RC22,RC24	For EMI request
03/17	31		Del RC2,RC3,CC7,CC8	For EMI request
03/20	13		Change C213 from SE070104Z80 to SE000000K80.	For prevent noise coupling
03/20	13		Change C231 from SE071101J80 to SE000000K80.	For prevent noise coupling
03/23	25		Change D18 BOM structure to @.	For EMI remove

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